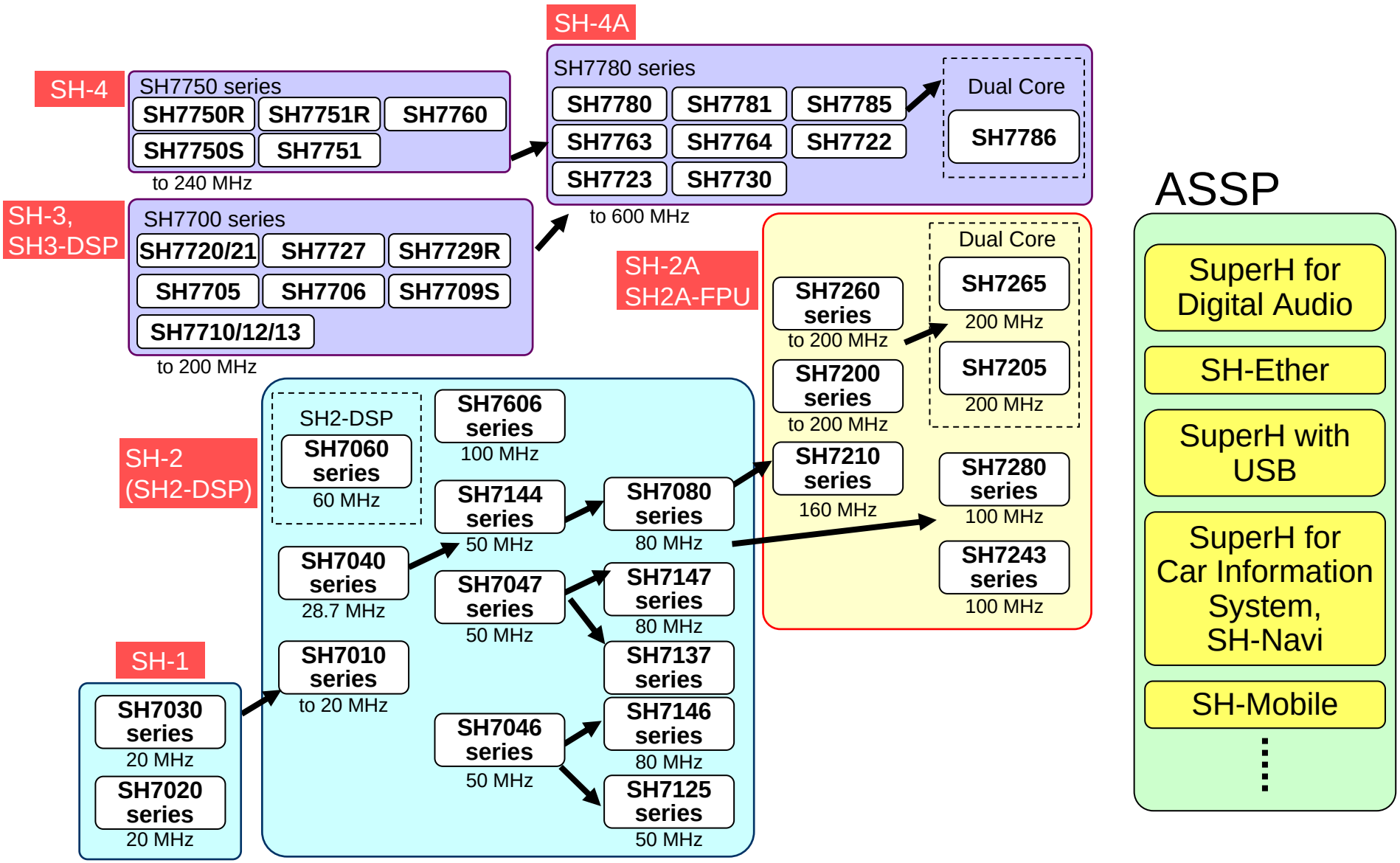
Renesas Microcomputers General Presentation

SuperH RISC engine Family

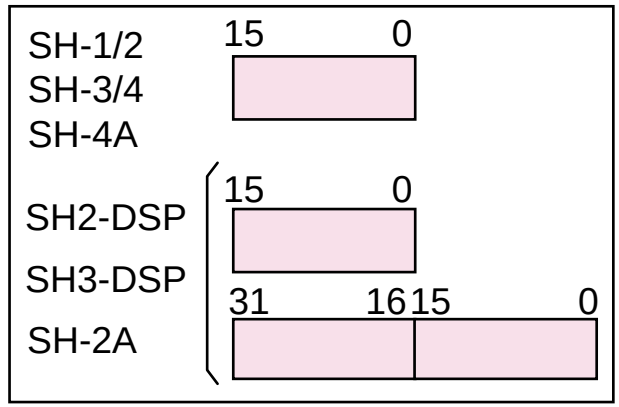
Renesas Technology Corp.

4/28/2009 Rev.16.00

SuperH RISC engine Roadmap



SuperH Instruction System



SH2-DSP
154 instructions
for DSP

SH3-DSP
160 instructions
MMU control instruction, etc.
instruction for DSP

SH-1
56 instructions

SH-2
62 instructions
32-bit multiply-and-accumulation, etc.

SH-3
68 instructions
MMU control instruction, etc.

SH-4
94 instructions
Floating-point instruction (single/double precision), etc.

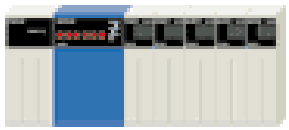
SH-4A
103 instructions
Floating-point instruction, cache operation instruction, etc.

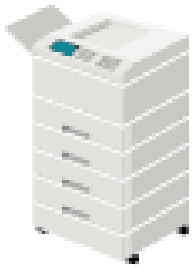
SH-2A
91 instructions
Enhanced shift, operation, bit manipulation, and division instructions

SH2A-FPU
112 instructions
Floating-point instruction (single/double precision)

Background of SH-2A Development

- Demands of Automotive, Industrial, and Consumer Appliances Fields -





- High-speed, highly-functional operations due to complex compound control
- High-speed control of mechanical sections such as external I/O module
- Improved real-time performance

- Increased ROM capacity
  - Reduction of program code size
- Better cycle performance
  - Instruction execution time (CPI) improvement
- High-speed response and improved real-time performance
  - Shorter interrupt response time

Features of the SH-2A

- Improved execution cycle performance
  - Harvard architecture (prevention of IF-MA contention)
  - 5-stage pipeline deferred
    - Prevention of increase in branch penalty and data hazard
  - Superscalar architecture
    (two instructions are issued simultaneously)
  - New instructions (32-bit + 16-bit instructions) added
- Improved interrupt response time
  - Introduction of register banks
- Reduced program code size
  - New instructions (32-bit + 16-bit instructions) added
    Improved code efficiency together with optimization by compiler

SH-2A: Most Powerful Real-Time Control Engine

1. Fastest interrupt response time

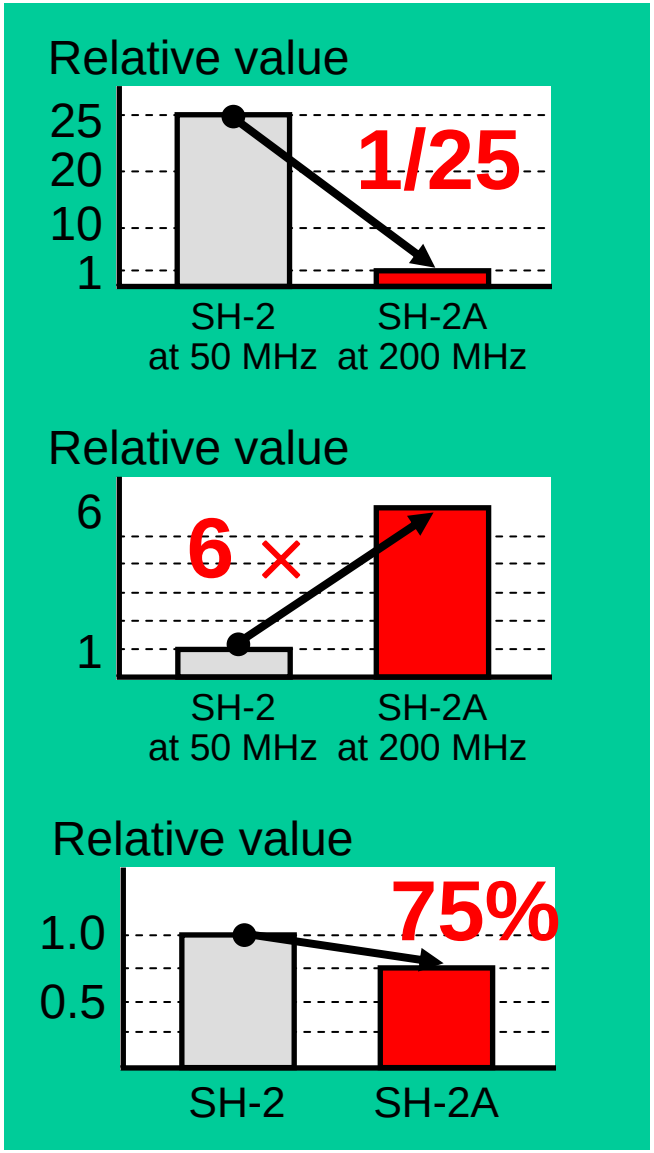
- Shortest interrupt response time:
  6 clock cycles (30 ns at 200 MHz)
- On-chip memory for saving register contents

2. Significantly-improved performance

- 1.5 times the performance of the SH-2
  at the same operation frequency
- Adoption of superscaler architecture
  (two instructions are simultaneously executed)

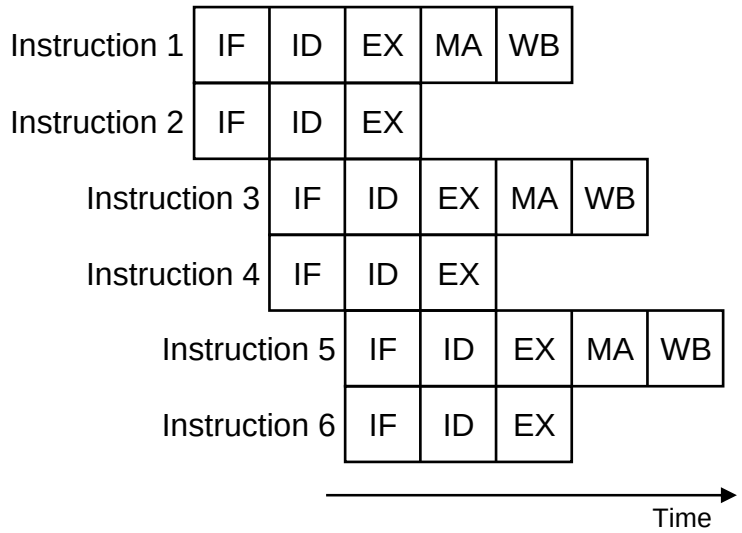
3. Greatly-improved code efficiency

- 1.3 times the code efficiency of the SH-2
  Efficiency in code size: 75% compared to the SH-2
- Addition of new instructions and improved compiler performance



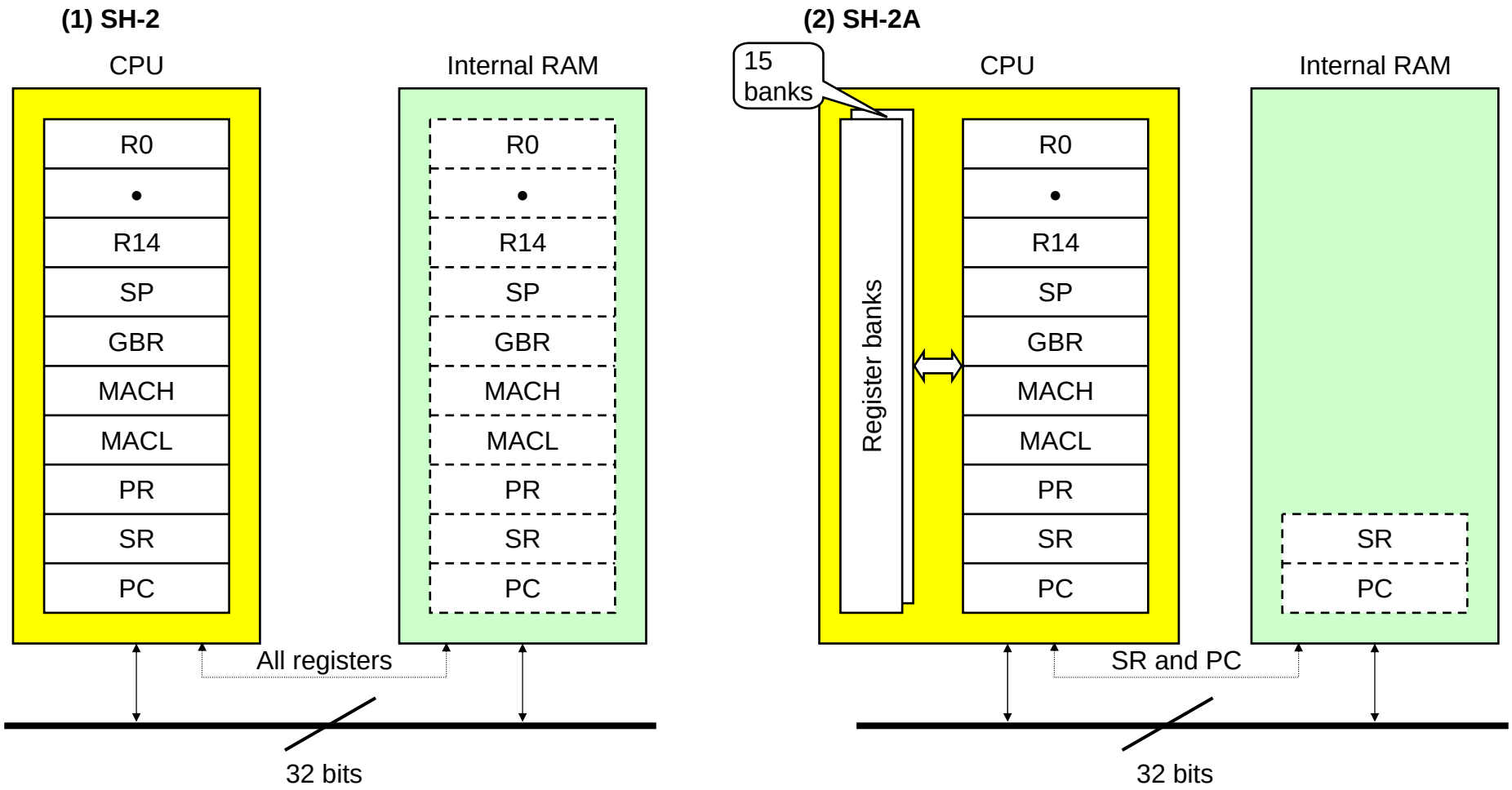
SH-2A Pipeline Operation

In the SH-2A, an instructions is executed by five-stage pipeline as shown below.
Two instruction are simultaneously issued by superscalar operation.



IF: Instruction fetch
ID: Decode
EX: Execution
MA: Memory access
WB: Write back

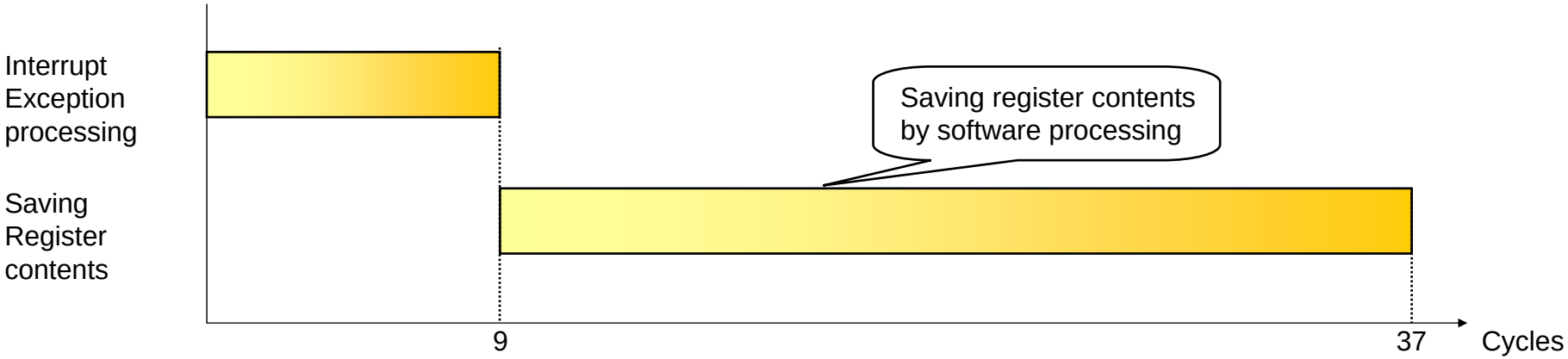
SH-2A Interrupt Latency Improvement (1)



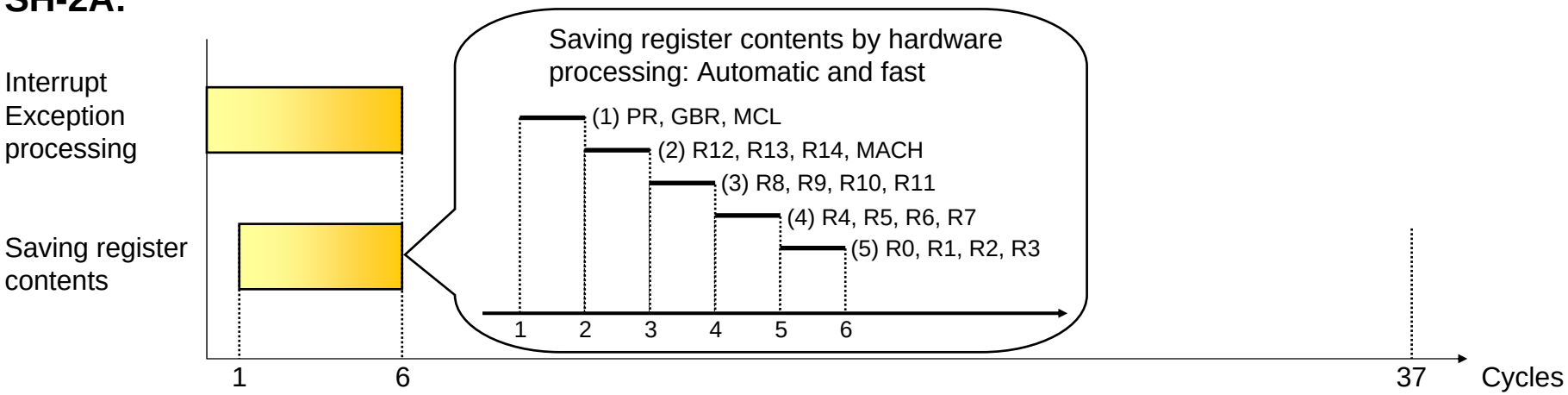
The SH-2A has memory for saving register contents according to interrupt priority level, which enables automatic and collective saving of register contents when an interrupt occurs.

SH-2A Interrupt Latency Improvement (2)

SH-2:



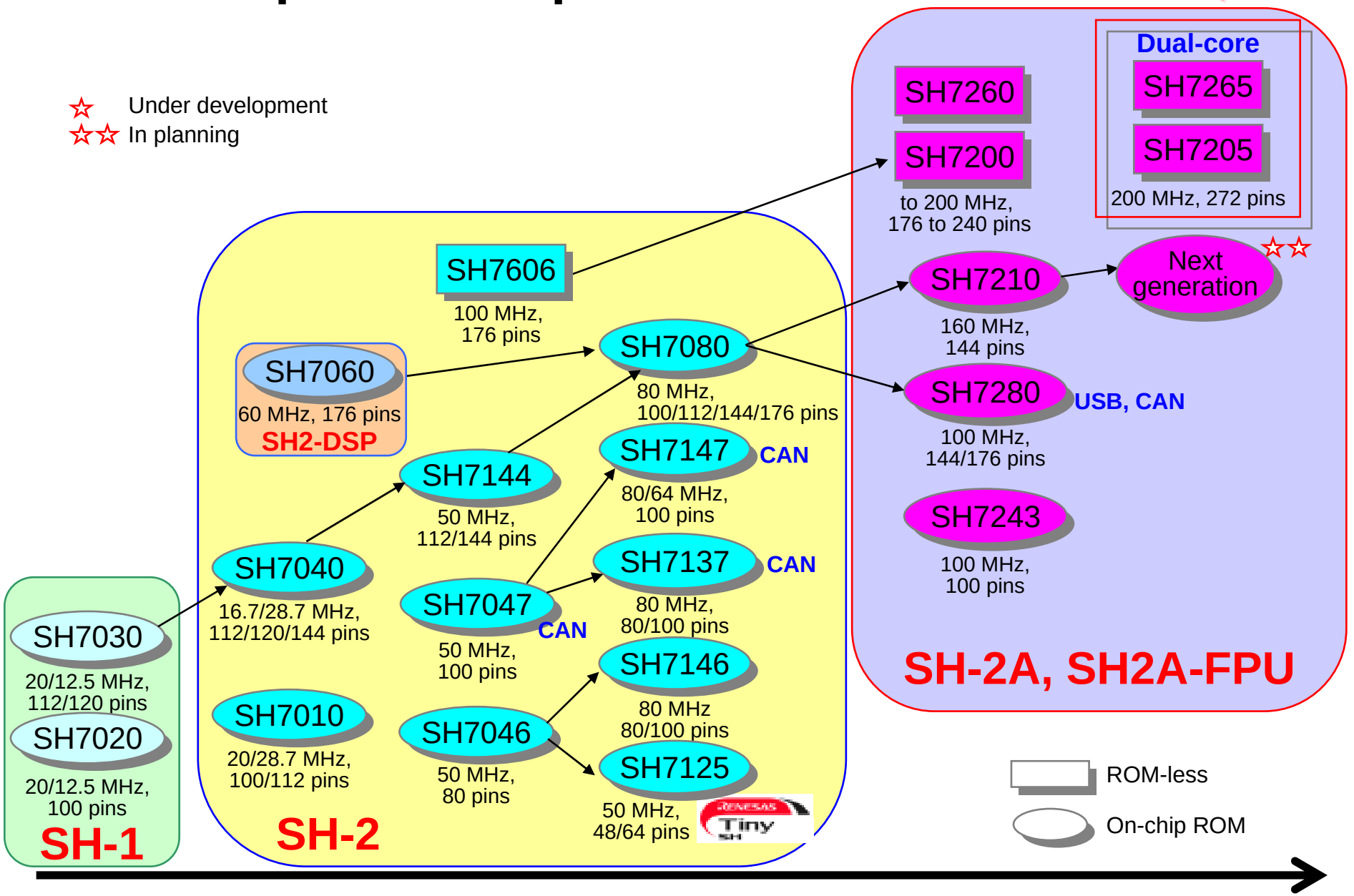
SH-2A:



Controller Type

SH7020 Series	SH7046 Series	SH7137 Series
SH7030 Series	SH7047 Series	SH7200 Series
SH7040 Series	SH7125 Series	SH7260 Series
SH7010 Series	SH7146 Series	SH7210 Series
SH7060 Series	SH7080 Series	SH7280 Series
SH7144 Series	SH7147 Series	SH7243 Series

Roadmap of the SuperH Controllers



Features of the SH7280 Series

Products in the SH7280 Series of flash-memory-equipped microcontrollers feature the new SH-2A CPU core and operate at a maximum frequency of 100 MHz.
As well as A/D converters with a 12-bit resolution and timers for motor control, on-chip peripheral modules include a USB interface.

- High performance SH-2A core
  - Higher CPU performance with 200 MIPS@100 MHz
  - Faster response to interrupts → On-chip register bank
- On-chip large-capacity flash memory: 512 KB/768 KB/1 MB
- Wide range of power-supply voltage: 3.0 to 5.5 V*
- Abundant peripheral modules
  - On-chip timers for advanced three-phase motors: MTU2 and MTU2S
  - High-speed A/D converters with 12-bit resolution: 1 μs/ch
  - Full-speed USB 2.0: 1
- On-chip debugging functionality
  - Full ICE and on-chip debugger

* Analog power: AVcc = 4.5 to 5.5 V
USB power: DrVcc = 3.0 to 3.6 V

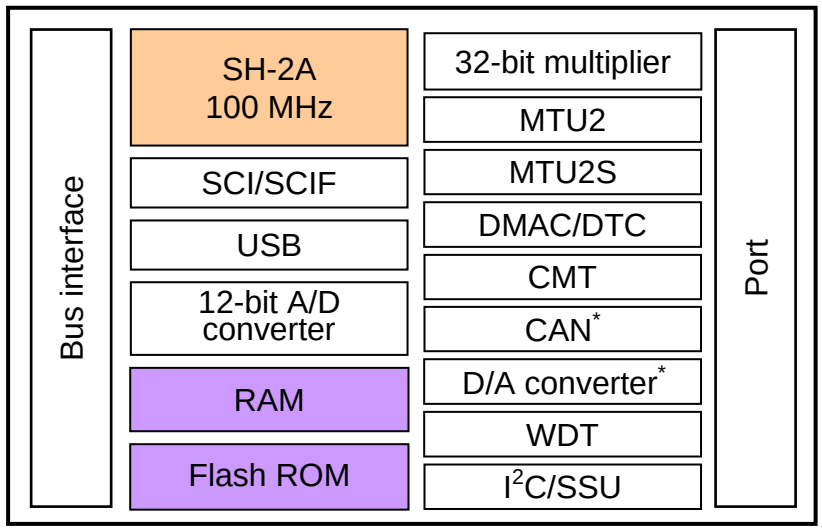
Main target applications

- Digital audio and visual devices, office equipment, card readers, general-purpose inverters, AC servomotors, numerically controlled machines, sequencers

Functional Overview of the SH7280 Series

- CPU core
  - SH-2A: SuperH RISC engine
  - 32-bit multiplier (32 bits × 32 bits = 64 bits)
  - Harvard architecture
- Operating frequency
  - CPU clock: 100 MHz (max.)
  - Bus clock: 50 MHz (max.)
  - Peripheral clock: 50 MHz (max.)
- Power-supply voltage
  - 3.0 to 5.5 V
    (AVcc = 4.5 to 5.5 V, DrVcc = 3.0 to 3.6 V)
- On-chip memory
  - Flash memory: 512 KB/768 KB/1 MB
  - RAM: 24 KB/32 KB
- External memory interfaces
  - SRAM, byte-selectable SRAM, burst ROM, SDRAM
  - External bus width
    - SH7285: 8 bits/16 bits
    - SH7286: 8 bits/16 bits/32 bits
  - External memory space is divisible into up to 8 areas (maximum 64-MB each).
- Packages
  - SH7285: LQFP-144 (20 mm × 20 mm, 0.5-mm pitch)
  - SH7286: LQFP-176 (20 mm × 20 mm, 0.4-mm pitch), LQFP-176 (24 mm × 24 mm, 0.5-mm pitch)
- On-chip function
  - 16-bit multi-function PWM timers: 6 (MTU2), 3 (MTU2S)
  - Port output enable (POE)
  - 16-bit peripheral timers: 2
  - Watchdog timer: 1
  - I^2C bus interface: 1
  - SSU interface: 1

- On-chip function
  - USB interface: 1, 2.0 Full Speed Function
  - RCAN-ET: 1 (only for the SH7286)
  - High-speed SCI: 1
    (16-stage transmission/reception FiFo)
  - SCI: 4
    (dual use as UART or clock synchronous)
  - Pins used for external interrupts: 9
  - DMA controller: 8 ch; DTC also included
  - 12-bit A/D converters
    - SH7285: 4 ch (with three S/H circuits) × 2 units
    - SH7286: 4 ch (with three S/H circuits) × 3 units
  - 8-bit D/A converters: 2 ch (only for the SH7286)
- On-chip debugging function
  - H-UDI/AUD
  - User break controller (UBC)



Block Diagram of the SH7280

*: SH7286 only.

Features of the SH7243 Series

Products in the SH7243 Series of flash-memory-equipped microcontrollers will feature the new SH-2A CPU core and operate at a maximum frequency of 100 MHz.
The SH7243 Series is derived from the SH7280 Series by trimming functionality (less on-chip ROM and RAM, USB, SSU, and other modules removed)for an initial product in a 100-pin package.

- High performance with SH-2A core
  - Higher CPU performance with 200 MIPS@100 MHz
  - Faster response to interrupts → On-chip register bank
- Wide range of power-supply voltage: 3.0 to 5.5 V*
- Abundant peripheral modules
  - On-chip timers for advanced three-phase motors: MTU2 and MTU2S
  - High-speed A/D converters with 12-bit resolution: 1 μs/ch
- On-chip debugging functionality
  - Full ICE and on-chip debugger

* Analog power: AVcc = 4.5 to 5.5 V

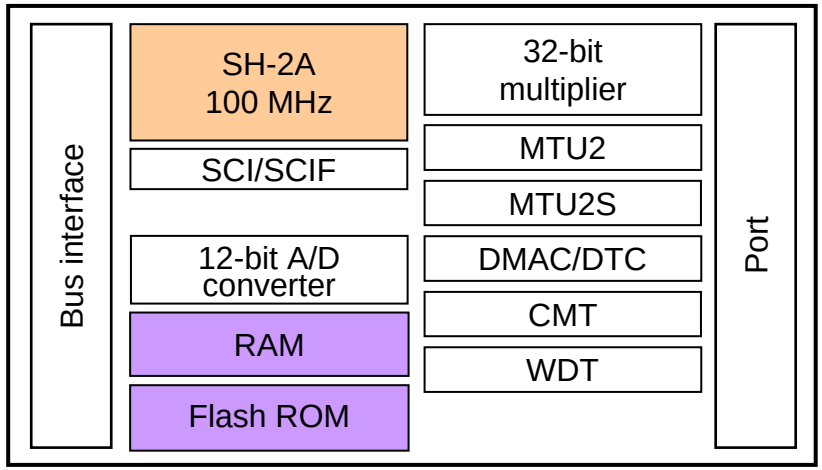
Main target applications

- AC servomotors, numerically controlled machines, sequencer, general-purpose inverters, robots, measuring equipment

Functional Overview of the SH7243 Series

- CPU core
  - SH-2A: SuperH RISC engine
  - 32-bit multiplier (32 bits × 32 bits = 64 bits)
  - Harvard architecture
- Operating frequency
  - CPU clock: 100 MHz (max.)
  - Bus clock: 50 MHz (max.)
  - Peripheral clock: 50 MHz (max.)
- Power-supply voltage
  - 3.0 to 5.5 V (AVcc = 4.5 to 5.5 V)
- On-chip memory
  - Flash memory: 128 KB/256 KB
  - RAM: 8 KB/12 KB
- External memory interfaces
  - SRAM, byte-selectable SRAM, burst ROM, SDRAM
  - External bus width: selectable as 8 bits/16 bits
- Package
  - LQFP-100 (14 mm × 14 mm, 0.5-mm pitch)
- On-chip peripheral function
  - 16-bit multi-function PWM timers:
    6 (MTU2), 3 (MTU2S)
  - Port output enable (POE)
  - 16-bit cycle timers: 2
  - Watchdog timer: 1

- On-chip peripheral function
  - High-speed SCI: 1
    (16-stage transmission/reception FiFo)
  - SCI: 2
    (dual use as UART or clock synchronous)
  - Pins used for external interrupts: 9
  - DMA controller: 8 ch; DTC also included
  - 12-bit A/D converters:
    4 ch (with three S/H circuits) × 2 units
- On-chip debugging function
  - H-UDI/AUD
  - User break controller (UBC)



Block Diagram of the SH7243

Features of the SH7210 Series

Products in the SH7210 Series of flash-memory-equipped microcontrollers feature the new SH-2A CPU core and operate at a maximum frequency of 160 MHz. On-chip peripheral modules include timers for motor control, A/D converters with a 12-bit resolution, etc.

- High performance SH-2A core
  - Higher CPU performance with 320 MIPS@160 MHz
  - Faster response to interrupts → On-chip register bank
- On-chip large-capacity flash memory: 512 KB/384 KB
- Abundant peripheral modules
  - On-chip timers for advanced three-phase motors: MTU2 and MTU2S
  - High-speed A/D converters with 12-bit resolution: 1.25 μs/ch
  - SDRAM interface
- On-chip debugging functionality
  - Full ICE and on-chip debugger

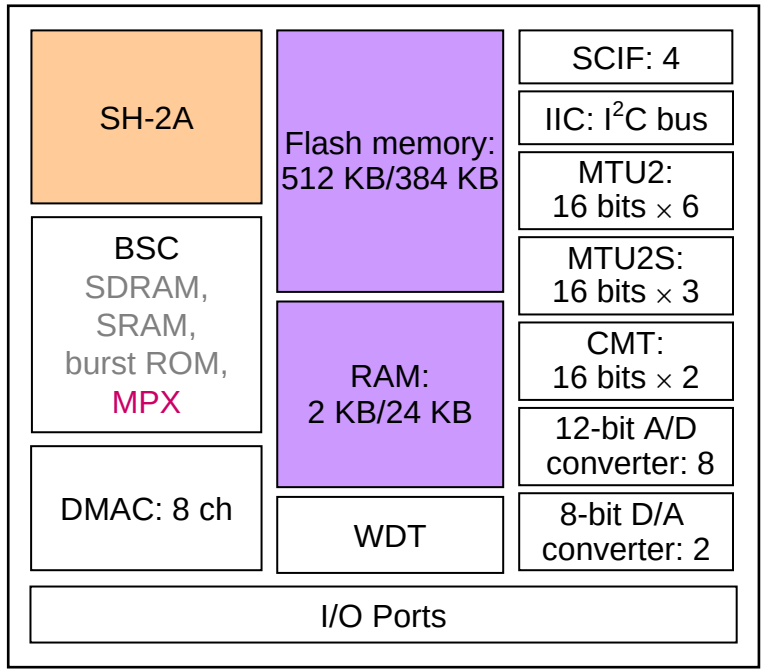
Main target applications

- AC servomotors, inverters, vending machines, surveillance cameras, video printers, bar-code readers, printers, color photocopiers

Functional Overview of the SH7210 Series

- CPU core
  - SH-2A: SuperH RISC engine
  - 32-bit multiplier (32 bits × 32 bits = 64 bits)
  - Harvard architecture
- Operating frequency
  - CPU clock: 160 MHz (max.)
  - Bus clock: 40 MHz (max.)
  - Peripheral clock: 40 MHz (max.)
- Power-supply voltage
  - 1.5 V ±0.1 V (CPU), 3.3 V ±0.3 V (I/O), 5.0 V ±0.5 V (A/D converter)
- On-chip memory
  - Flash memory: 512 KB/384 KB
  - RAM: 32 KB/24 KB
- External memory interfaces
  - SRAM, byte-selectable SRAM, burst ROM, SDRAM
  - External bus width: 8 bits/16 bits
- Package
  - LQFP2020-144 (0.5-mm pitch)
- On-chip peripheral function
  - 16-bit multi-function PWM timers: 6 (MTU2), 3 (MTU2S)
  - Port output enable (POE)
  - 16-bit cycle timers: 2
  - Watchdog timer: 1
  - I^2C bus interface: 1
  - High-speed SCI: 4 (16-stage transmission/reception FiFo)
  - DMA controller: 8 ch
  - 12-bit A/D converters: 8 ch (with three S/H circuits)
- On-chip peripheral function
  - 8-bit D/A converters: 2 ch
- On-chip debugging function
  - H-UDI/AUD
  - User break controller (UBC)

Block Diagram of the SH7211



Part no.	Range of operating temperature
R5F72115D160FPV	-40 to +85 °C

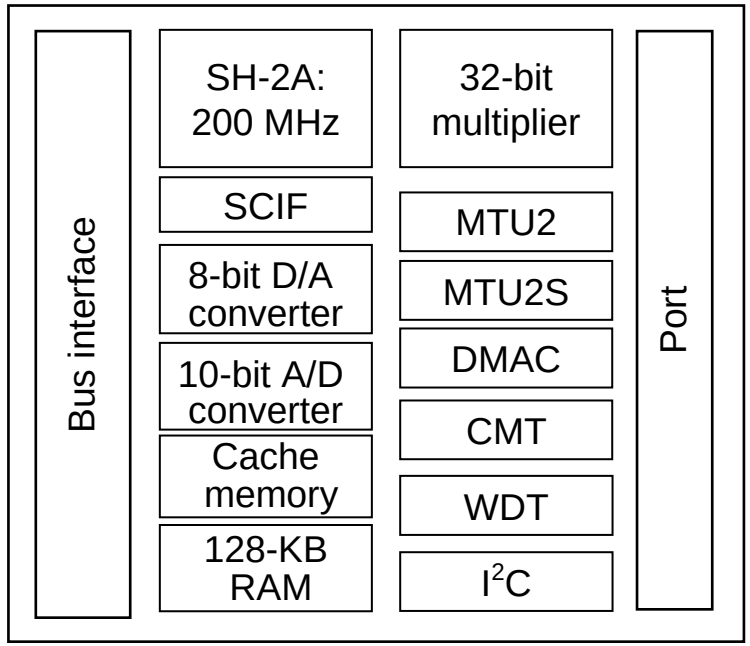
Functions and Features of SH7206

- High-performance SH-2A CPU core
  - Equivalent to SH-4 → 480 MIPS@200 MHz
  - Faster response to interrupts → internal register banks
- Low-power consumption and high performance: 2560 MIP software
- Large-capacity RAM: 128-KB/200-MHz access
- On-chip data/instruction separation cache: Total 16 KB
- Abundant bus interface
  - SDRAM I/F, PCMCIA
  - Burst ROM I/F, etc.
- On-chip peripheral functions for real time control
  - Multi-functional timer: 16 bits × 11 ch, motor control
  - Various analog input/output: 10-bit A/D converter, 8-bit D/A converter

Overview of the SH7206

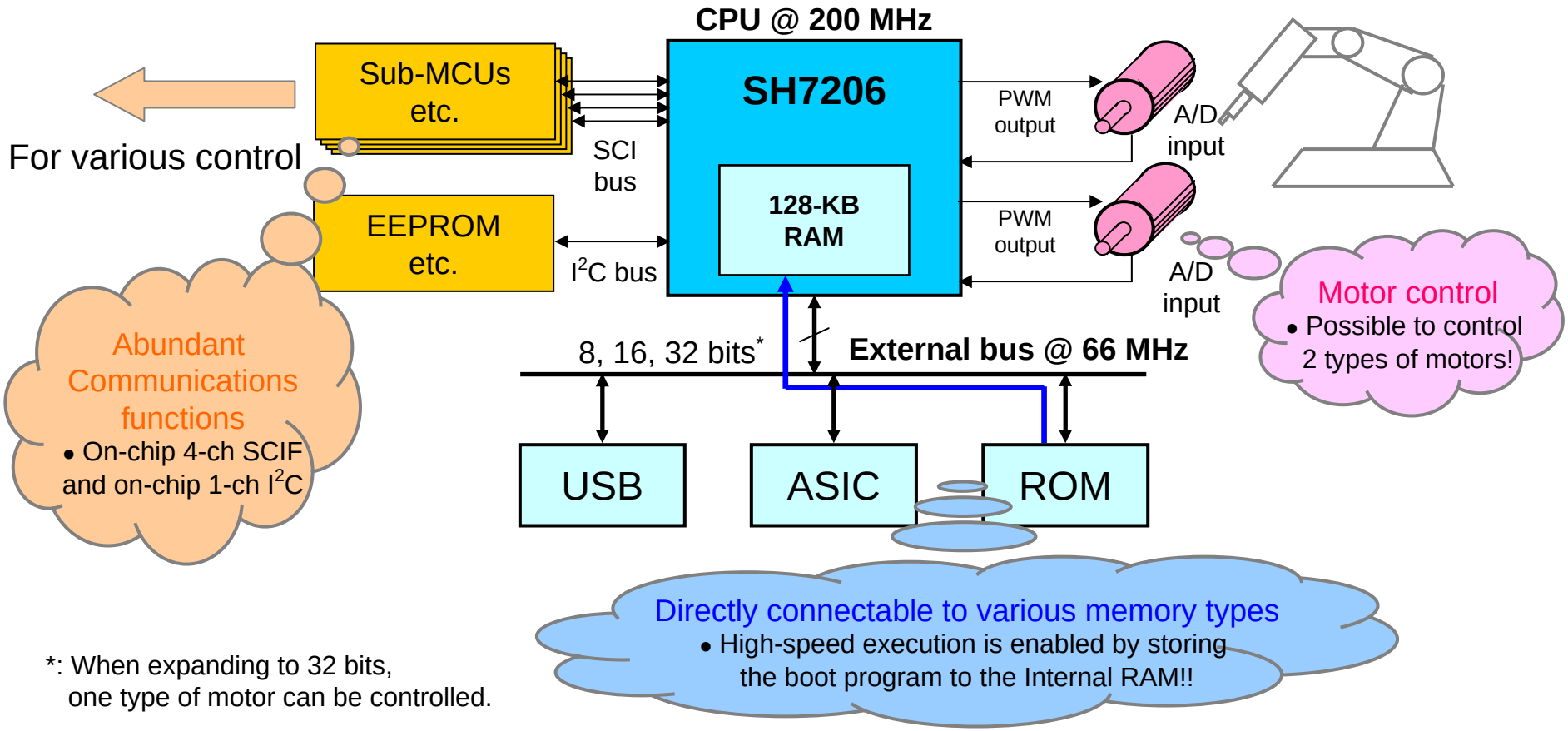
- CPU core
  - SH-2A (SuperH RISC engine)
  - 32-bit on-chip multiplier (32 bits × 32 bits → 64 bits)
  - Harvard architecture
- Operating frequency
  - CPU clock: 200 MHz (max.)
  - Bus clock: 66 MHz (max.)
  - Peripheral clock: 33 MHz (max.)
  - Clock dedicated for the MTU2S: 100 MHz (max.)
- Power supply voltage
  - 3.0 to 3.6 V and 1.15 to 1.35 V (analog power supply: 3.0 to 3.6 V)
- Internal memory
  - 32 KB RAM × 4 mat: a total of 128 KB
  - Instruction cache: 8 KB
  - Operand cache: 8 KB
- External memory interface
  - SRAM, byte selectable SRAM, multiplexed I/O, PCMCIA, burst ROM
  - External bus width: selectable from 8 bits, 16 bits, or 32 bits
  - External memory spaces can be divided into 9 spaces (576 Mbytes at maximum)
- Package
  - LQFP-176 (24 mm square, 0.5 mm pitch)
- Internal functions
  - Multifunctional 16-bit PWM timer: 6 (MTU2) and 3 (MTU2S)
  - Port output enable (POE): 9

- Internal functions
  - 16-bit cycle timer: 2
  - Watchdog timer (WDT): 1
  - I^2C bus interface: 1
  - DMA controller: 8 ch
  - 10-bit A/D converter: 4 ch × 2
  - 8-bit D/A converter: 2 ch
  - SCIF: 4 (16-stage built-in FIFO for transmit and receive operations)
  - I/O port: 81
  - External interrupt pin: 17
  - JTAG interface



Example: AC Servo System Configuration Using SH7206

- Achieves maximum CPU performance by having programs resident in internal RAM.
- On-chip cache improves the performance of externally installed programs.
- Abundant functions such as three-phase PWM output timeaaar, 10-bit A/D converter, and more.



*: When expanding to 32 bits, one type of motor can be controlled.

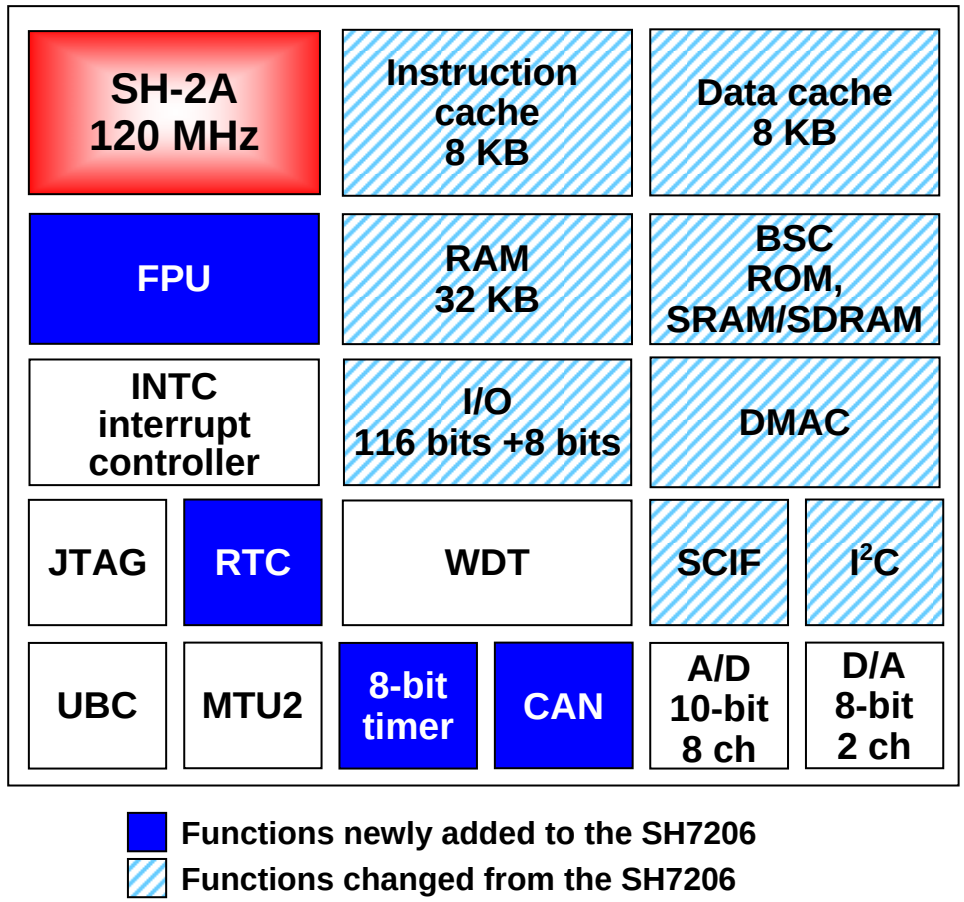
SH7201 Functions and Features

- Incorporates high-performance SH-2A core
  - CPU performance equivalent to the SH-4 → 288 MIPS@120 MHz
  - High-speed response to interrupt processing → On-chip register bank
- On-chip double-precision FPU
  - Realizes signal processing performance higher than the DSP
  - Enhances software development by the FPU
    (eliminates digit alignment processing)
- Abundant interfaces such as CAN and I^2C-bus
- Rich set of bus interface
  - SDRAM interface
  - Burst ROM interface, etc.
- Internal peripheral functions for realtime control
  - Many on-chip timers: 16 bits × 11 ch, motor control is possible
  - Ample analog input/output 10-bit A/D converter, 8-bit D/A converter

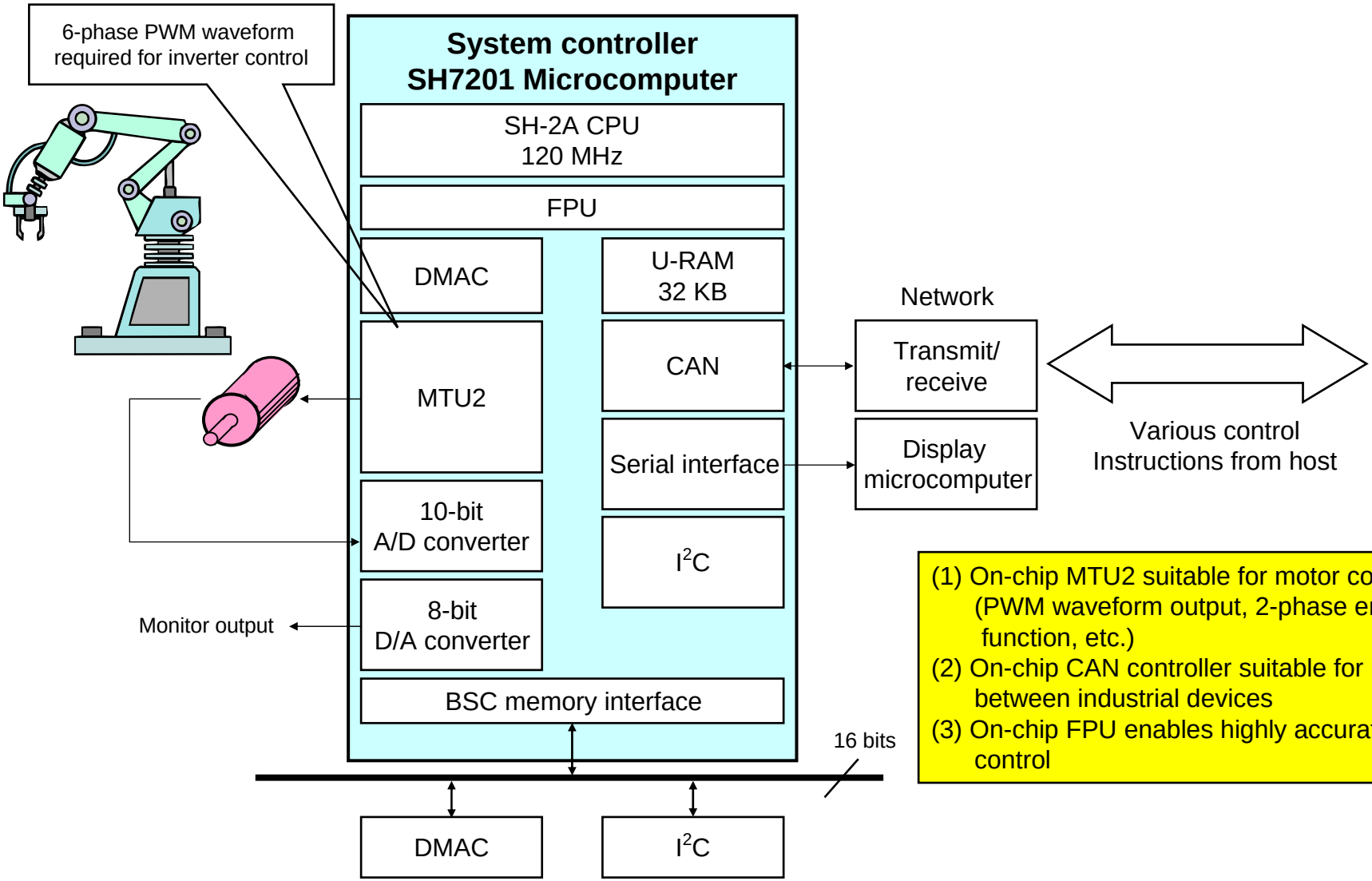
Overview of the SH7201

- CPU core
  - SH-2A (SuperH RISC engine) FPU
  - 32-bit multiplier (32 bits × 32 bits → 64 bits)
  - Harvard architecture
- Operating frequency
  - CPU clock: 120 MHz (max.)
  - Bus clock: 60 MHz (max.)
  - Peripheral clock: 40 MHz (max.)
- Power-supply voltage
  - 3.0 to 3.6 V
- Internal memory
  - RAM: 32 KB
  - Instruction cache: 8 KB
  - Operand cache: 8 KB
- External memory interface
  - SRAM, SDRAM interface
  - External bus width is selectable from 8, 16 bits or 32 bits
  - External memory spaces can be divided into 7 areas (64 MB max.)
- Internal functions
  - Multi-functional 16-bit PWM timer: 6 (MTU2)
  - 8-bit timer (waveform output): 2
  - Watchdog timer: 1
  - CAN interface: 2 (2.0A, 2.0B)
  - I^2C bus interface: 3
  - DMA controller: 8 ch (includes 4 ch for external requests)
  - 10-bit A/D converter: 4 ch × 2
  - 8-bit D/A converter: 2 ch
  - SCIF: 8 (16-stage transmit/receive FIFO included)
  - I/O port: I/O: 116, Input: 8
  - External interrupt pin: 17
  - JTAG interface

- Package
  - 176-pin LQFP (24-mm square, 0.5-mm pitch)



Industrial Measurement Device Application Example Using the SH7201



(1) On-chip MTU2 suitable for motor control (PWM waveform output, 2-phase encoder function, etc.)
(2) On-chip CAN controller suitable for interface between industrial devices
(3) On-chip FPU enables highly accurate current control

Functions and Features of the SH7203

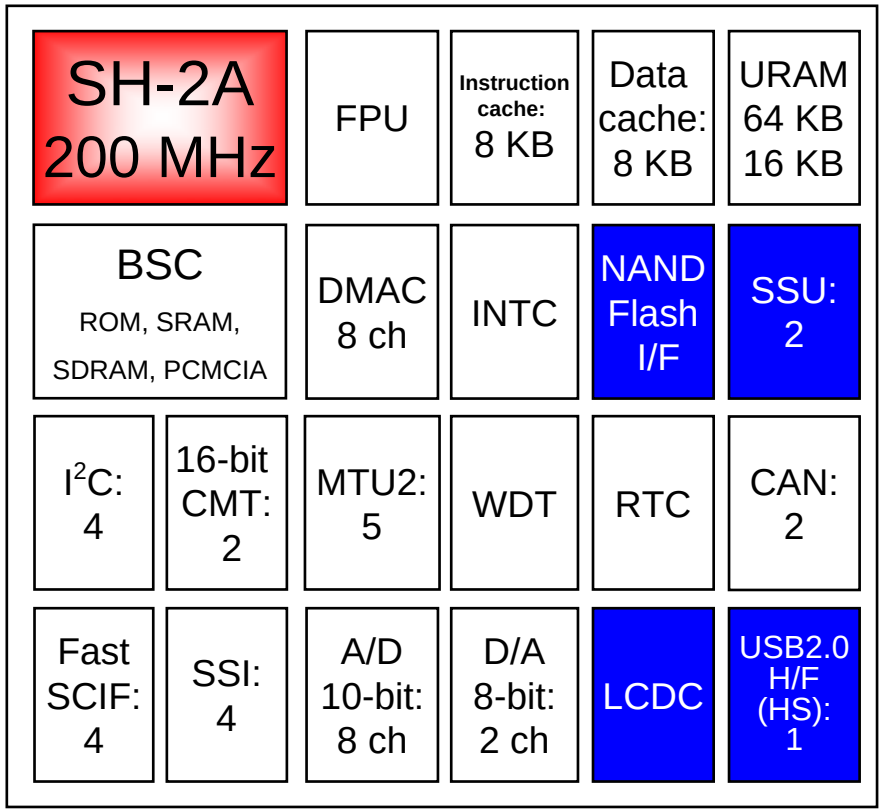
- High-performance SH-2A core
  - Performance comparable to an SH-4 CPU → 480 MIPS@200 MHz
  - Highly responsive interrupt processing → incorporation of register banks
- Double-precision FPU
  - Better signal-processing performance than a DSP
  - Simpler development of software using FPU (matching digits is not required.)
- On-chip module for USB v.2.0 standard high-speed Host and Function operation
  - Large amount of data transferable at high-speed
  - Switching between Host and Function
- Liquid crystal display controller handles displays up to WVGA size (800 × 480 pixels)
- Abundant communications interface functions
  - I^2C, CAN, serial with FIFO, SPI-compliant serial, serial for sound
- Multifunctional timer for motor control, A/D converter, D/A converter

Overview of the SH7203

- CPU core
  - SH-2A (SuperH RISC engine) FPU
- Operating frequency
  - CPU clock: 200 MHz (max.)
  - Bus clock: 66 MHz (max.)
- Power-supply voltage: dual power supply
  - Internal 1.2 V/external 3.3 V
- Internal memory
  - URAM: 64 KB
  - RAM with standby retention: 16 KB
  - Cache: I = 8 KB, D = 8 KB
- External memory interface
  - SRAM, SDRAM, PCMCIA interface
  - External data-bus width selectable as 8, 16, or 32 bits
  - External memory space can be divided into seven areas (64 MB max.)
- Internal functions
  - 16-bit multifunctional timer: 5 (MTU2)
  - 16-bit timer (CMT): 2
  - Watch dong timer: 1
  - CAN interfaces: 2 (2.0A, 2.0B)
  - I^2C bus interfaces: 4
  - DMA controller: 8 ch (includes 4 ch. that can be activated by external requests)
  - 10-bit A/D converter: 8 ch
  - SCIF: 4 (16-stage transmit/receive FIFO included)
  - SSI: 4
  - SSU: 2
  - USB2.0 (high speed): Host or Function selectable
  - NAND flash I/F
  - LCD controller
  - I/O ports
  - JTAG interface

- Package
  - 240-pin QFP

* Specifications are subject to change.



: Function added to the SH7201

SH7261 Functions and Features for Digital Audio Systems

- Using the SH-2A CPU (120 MHz performance) and FPU, decoding and encoding WMA, AAC, MP3, ATRAC3, etc. can be achieved by software
  - Eliminates external decoder chip
  - Multi-decoding is enabled

- Ripping an external USB memory or HDD player is possible
  - CPU encoding
  - Support for various encoder is in examination

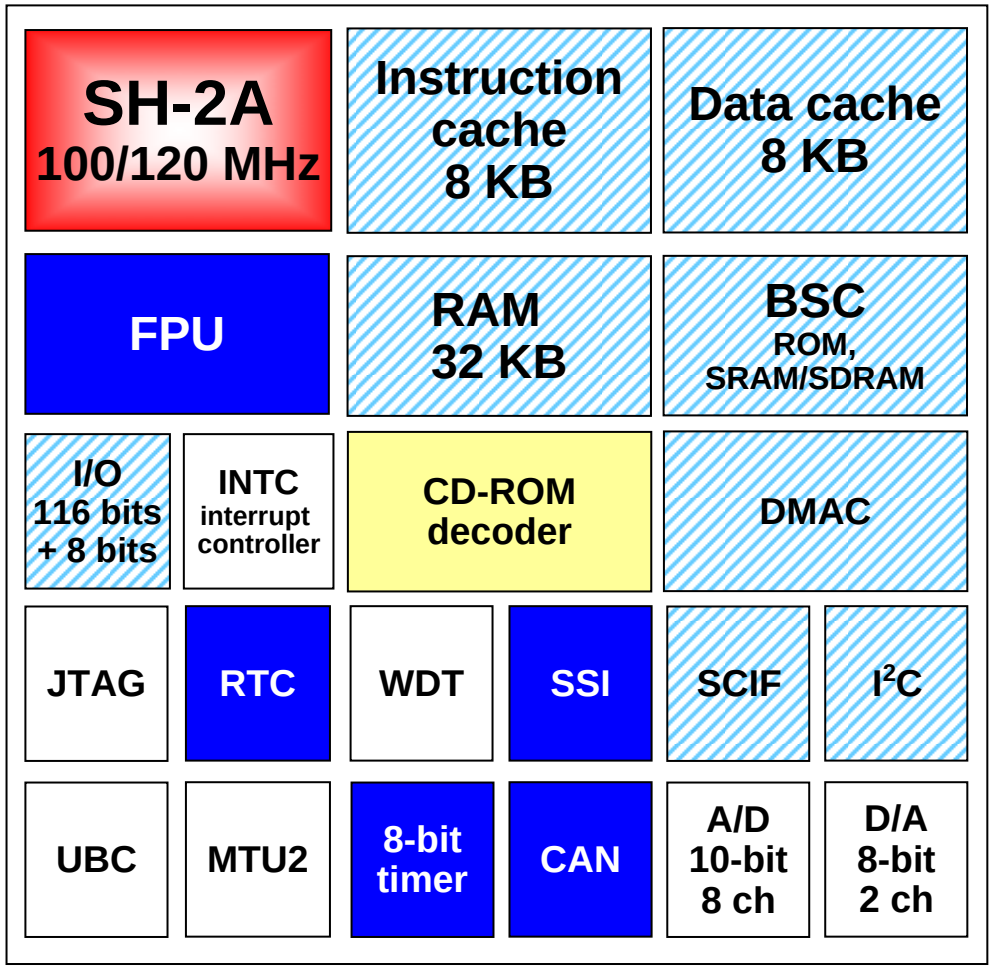
- On-chip CD-ROM decoder
  - External components can be eliminated

- Various on-chip interfaces such as CAN and audio interface (SSI)

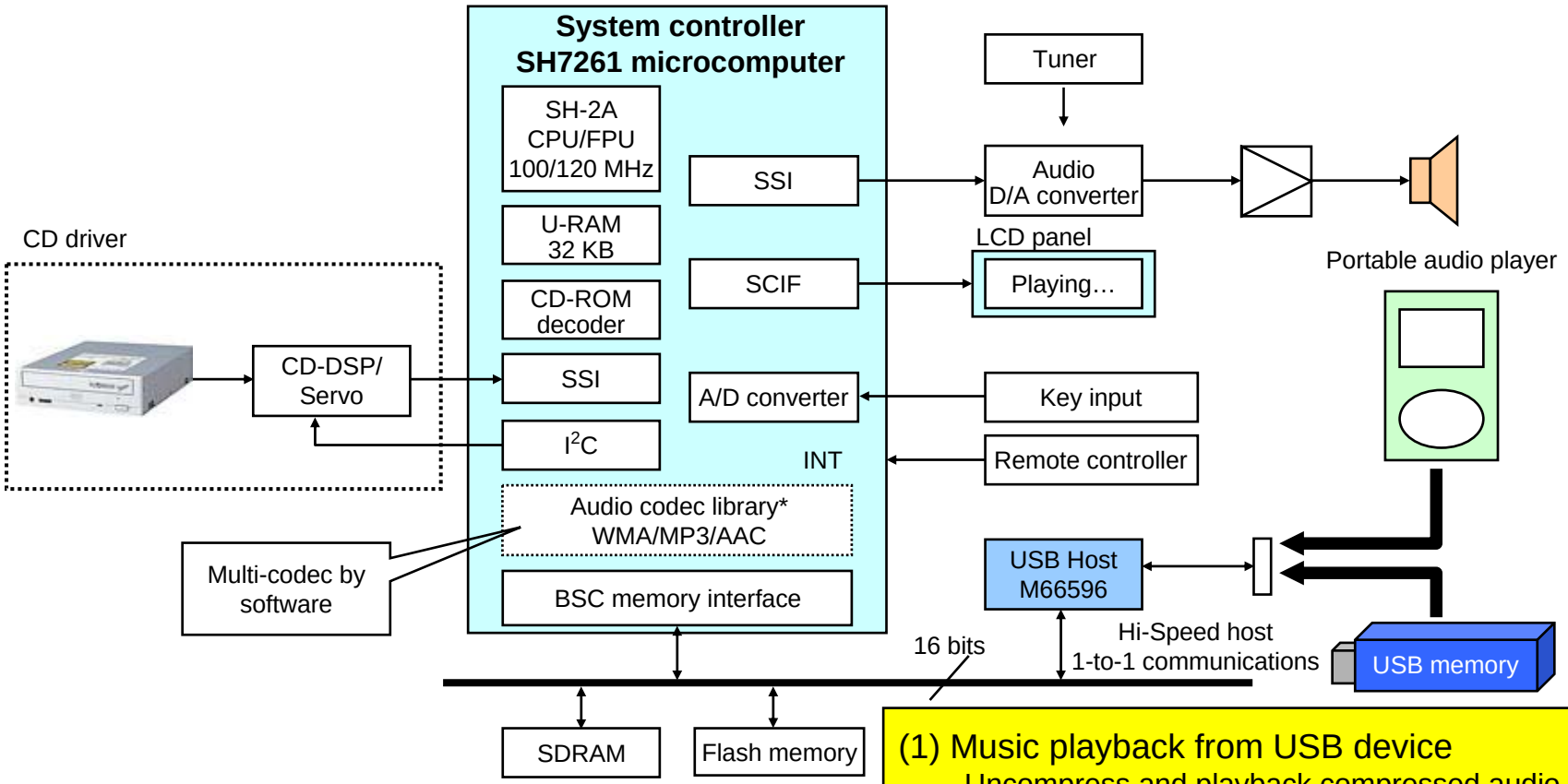
SH7261 Functional Outline

- CPU core
  - SH-2A (SuperH RISC engine)
  - On-chip 32-bit multiplier (32 bits × 32 bits → 64 bits)
- Operating frequency
  - CPU clock: 120 MHz (max.)
  - Bus clock: 60 MHz (max.)
  - Peripheral clock: 40 MHz (max.)
- Power-supply voltage
  - 3.0 to 3.6 V
- On-chip memory
  - RAM: 32 KB
  - Instruction cache: 8 KB
  - Operand cache: 8 KB
- External memory interface
  - SRAM, SDRAM interface
  - External bus width selectable from 8, 16, or 32 bits
  - External memory space can be divided into 7 (64 Mbytes max.) areas
- Internal functions
  - Multifunctional 16-bit PWM timer: 6 (MTU2)
  - 8-bit timer (waveform output): 2 ch
  - Watchdog timer: 1
  - CAN interface: 2 (2.0A, 2.0B)
  - I^2C bus interface: 3
  - DMA controller: 8 ch (includes 4 ch which external request is enabled)
  - 10-bit A/D converter: 4 ch × 2
  - 8-bit D/A converter: 2 ch
  - SCIF: 8 (16-stage transmit/receive FIFO included)
  - SSI: 2
  - CD-ROM decoder (Mode0/1/2/2Form1/2Form2)
  - I/O port: I/O: 116, Input: 8
  - External interrupt pin: 17
  - JTAG interface

- Package
  - 176-pin LQFP (24 mm square, 0.5-mm pitch)



Configuration Example of Digital Home Audio System Using the SH7261 Supporting USB Memory



(1) Music playback from USB device
Uncompress and playback compressed audio sound within USB memory or portable players

(2) CD ripping to USB device
Compress music CD data, and store them in USB memory or portable audio players

SH7263 Functions and Features for Digital Audio Systems

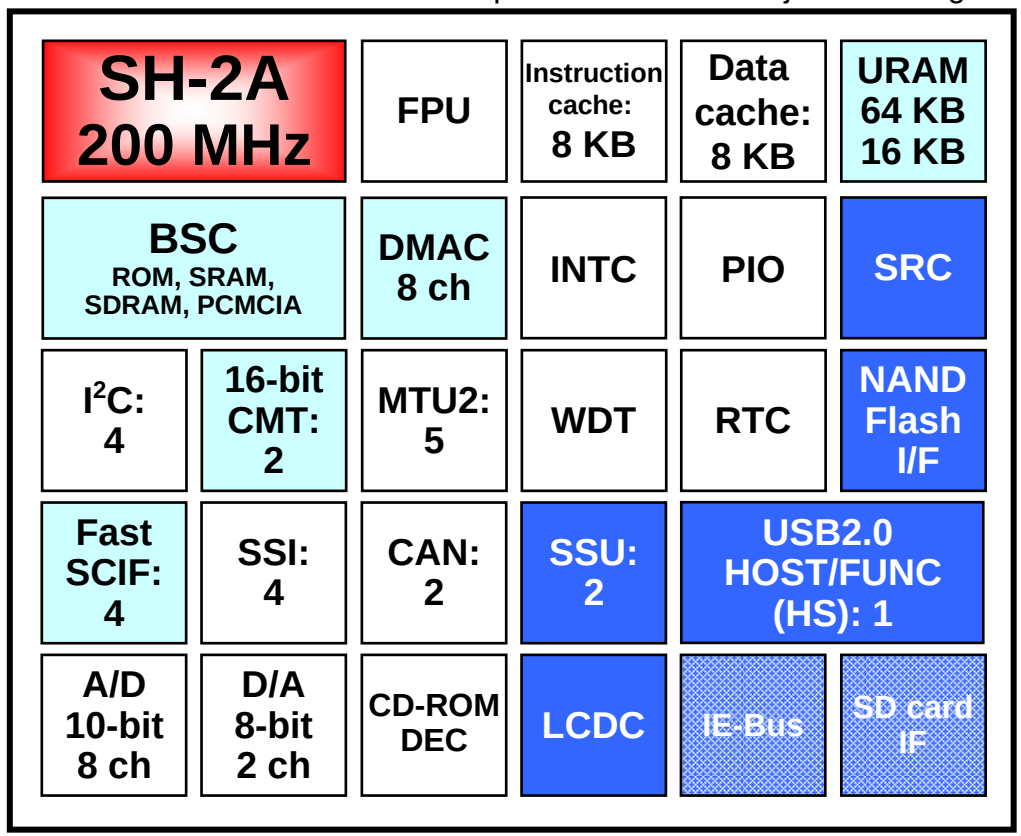
- High-performance SH-2A core
  - Performance comparable to an SH-4 CPU → 480 MIPS@200 MHz
  - Highly responsive interrupt processing → incorporation of register banks
- Double-precision FPU
  - Better signal-processing performance than a DSP
  - Decoding and encoding of WMA, AAC, and MP3 realizable in software
- On-chip module for USB v.2.0 standard high-speed Host and Function operation
  - Large amount of data transferable at high speeds
  - Switching between Host and Function
- Liquid crystal display controller handles displays up to WVGA size (800 × 480 pixels)
- Abundant communications interface functions
  - I^2C, CAN, serial with FIFO, SPI-compliant serial, serial for sound
- Internal functions for digital audio
  - CD-ROM decoder, sampling-rate converter, SD-card interface

Functional Overview of the SH7263

- CPU core
  - SH-2A (SuperH RISC engine) FPU
- Operating frequency
  - CPU clock: 200 MHz (max.)
  - Bus clock: 66 MHz (max.)
- Power-supply voltage: dual power supply
  - Internal 1.2 V/external 3.3 V
- Internal memory
  - URAM: 64 KB
  - RAM with standby retention: 16 KB
  - Cache: I = 8 KB, D = 8 KB
- External memory interfaces
  - SRAM, SDRAM, PCMCIA interface
  - External data-bus width selectable as 8, 16, or 32 bits
  - External memory space can be divided into seven areas (64 MB max.)
- Internal functions
  - 16-bit multifunctional timers: 5 ch (MTU2)
  - 16-bit timers (CMT): 2
  - Watchdog timer:1
  - CAN interfaces: 2 (2.0A, 2.0B)
  - I^2C bus interfaces: 4
  - DMA controller: 8 ch (includes 4 ch that can be activated by external requests)
  - 10-bit A/D converter: 8 ch
  - SCIF: 4 (16-stage transmit/receive FIFO included)
  - SSI: 4
  - SSU: 2
  - SRC (sampling-rate converter)
  - USB2.0 (high-speed): Host or Function selectable
  - SD-card interface
  - NAND flash I/F
  - CD-ROM decoder

- Internal functions
  - LCD controller (equivalent to that of the SH7760)
  - I/O ports
  - JTAG interface
- Package
  - 240-pin QFP

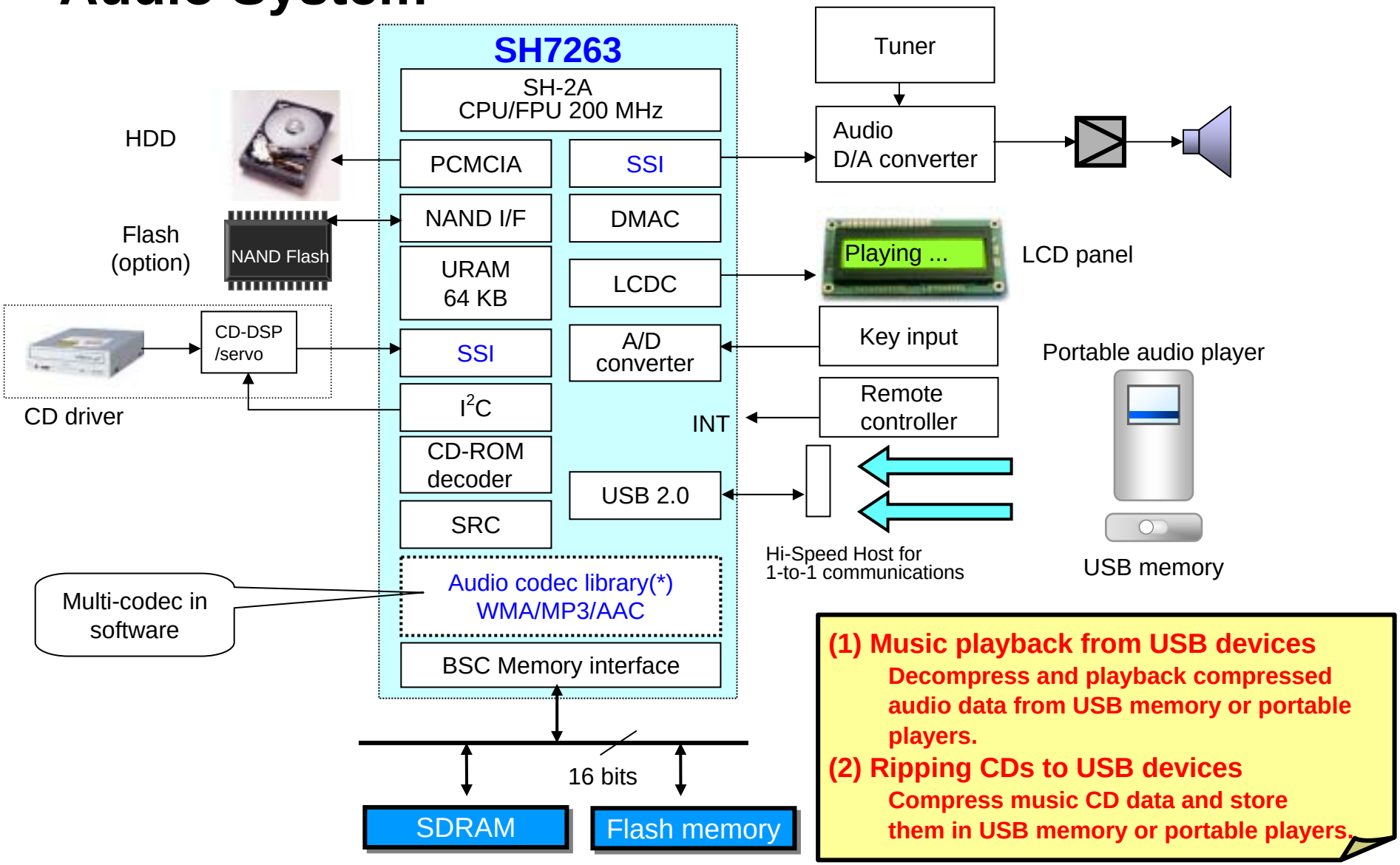
* Specifications are subject to change.



: Function added to the SH7261

: Function changed from the SH7261

Using the SH7263 for a USB-Supporting Audio System



(1) Music playback from USB devices

Decompress and playback compressed audio data from USB memory or portable players.

(2) Ripping CDs to USB devices

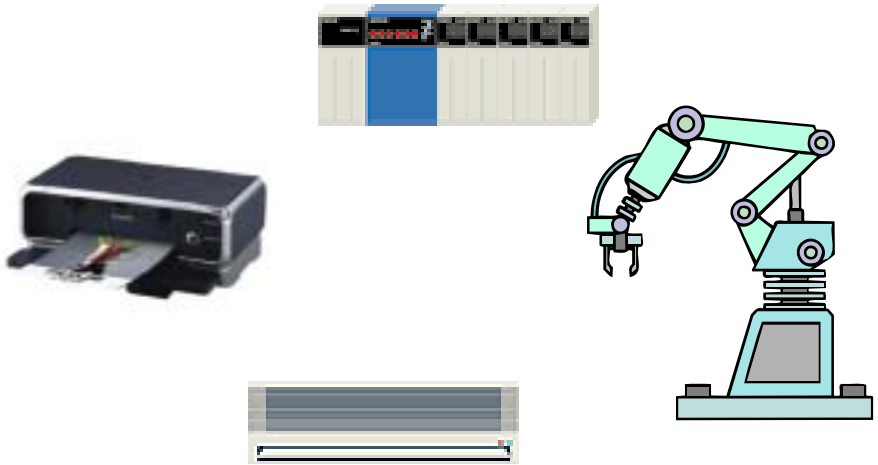
Compress music CD data and store them in USB memory or portable players.

Summary of the SH2A-DUAL Platform

- AMP: Asymmetric multiprocessor
- Application of the multi-layer bus (MLB), designed with an emphasis on low latency
  - Bus configuration with four independent layers:
    two for CPU use as bus masters, two for the DMAC
  - Two CPUs to act as the two bus masters
  - The MLB has been widely used as a standard bus for SoC (system on chip).
- On-chip SH2A-FPU (200 MHz) CPU cores suit embedded control systems.
  - The FPUs handle signal processing and calculations for industrial, music,
    and other applications.
  - Concomitant usage of URAM draws out greater effective performance.
  - Register banks enable faster response.
- Configurations that include internal flash memory will be available.
- Dual ITRON and debuggers
- We are working towards even better performance and power consumption.

Functional Overview of the SH7205

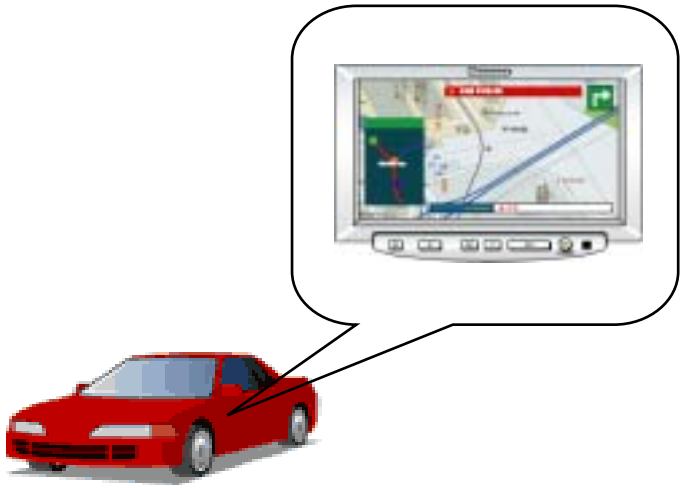
- Applications
  - Equipment and devices for industrial and general uses
- Abundant peripheral functional modules
  1. Supports various storage interfaces (ATAPI/NAND flash/USB 2.0)
  2. On-chip 2D engine (input of digital video, output of analog RGB)
  3. On-chip multi-functional timers: Facility for motor control
- Package:
  272-pin BGA (ball-grid array)



SH-2A (200 MHz)		FPU	Instruction cache: 8 KB	Data cache: 8 KB
SH-2A (200 MHz)		FPU	Instruction cache: 8 KB	Data cache: 8 KB
BSC ROM, SRAM, SDRAM		DMAC	URAM: 32 KB	URAM: 64 KB
MTU2: 5	INTC	SSI: 6	ATAPI	CAN: 2
10-bit A/D Converter: 8	WDT	NAND Flash IF	USB 2.0 HOST (HS) 2 ports/ FUNC (HS) 1 port	SCIF: 6
RTC	SSU: 2	2D Graphics		I^2C

Functional Overview of the SH7265

- Applications
  - Digital on-board equipment for vehicles, including car audio and car navigation systems
- Functional modules added to those of the SH7205
  1. SD-card interface
  2. IE Bus
  3. Handling of compressed music files (AAC format) Encoding accelerator
- Support for vehicle product quality (-40 to 85°C)
- Package
  272-pin BGA (Ball Grid Array)



SH-2A (200 MHz)		FPU	Instruction cache: 8 KB	Data cache: 8 KB
SH-2A (200 MHz)		FPU	Instruction cache: 8 KB	Data cache: 8 KB
BSC ROM, SRAM, SDRAM		DMAC	URAM 32 KB	URAM 64 KB
MTU2: 5	INTC	SSI: 6	SCIF: 6	CAN: 2
			USB 2.0 HOST (HS) : 2 ports/ FUNC (HS) : 1 port	
10-bit A/D Converter: 8	WDT	NAND Flash IF	**SD Card IF**	I^2C
RTC	SSU: 2	2D Graphics	**AAC Enc.**	ATAPI
				IE Bus

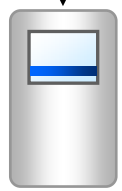
: Difference from the SH7205

Example of an Application for Music Playback and CD Encoding

- A CD drives are connectable to the PC-ATA driver or the SSI interface (4 × read CD-ROM drive).

- I/O functions for video allow for display of external video.
- Two USB 2.0 (HS) ports are available

ATA
I²C
2D Graphics
RGB
A2D IC
RGB
TFT Monitor QVGA
AAC Encoder
SH-2A CPU/FPU 200 MHz
A/D
Touch panel
SD IF
SH-2A CPU/FPU 200 MHz
USB 2.0 (HS)
2 Ports
USB
USB Connector
Hub
USB Connector
Hub
Bus I/F ROM, SRAM, SDRAM
Video
IIS (SSI)
D/A
Flash
SDRAM



Decompression and playback of compressed audio data:
the SH-2A CPU is capable of decompressing and playing back compressed audio data in several formats (MP3/WMA/AAC codecs are available).
Compression of audio data:
The SH-2A CPU can handle software compression (MP3/AAC) or use the AAC encoder.

Features of the SH7262 and SH7264

SH7262/SH7264

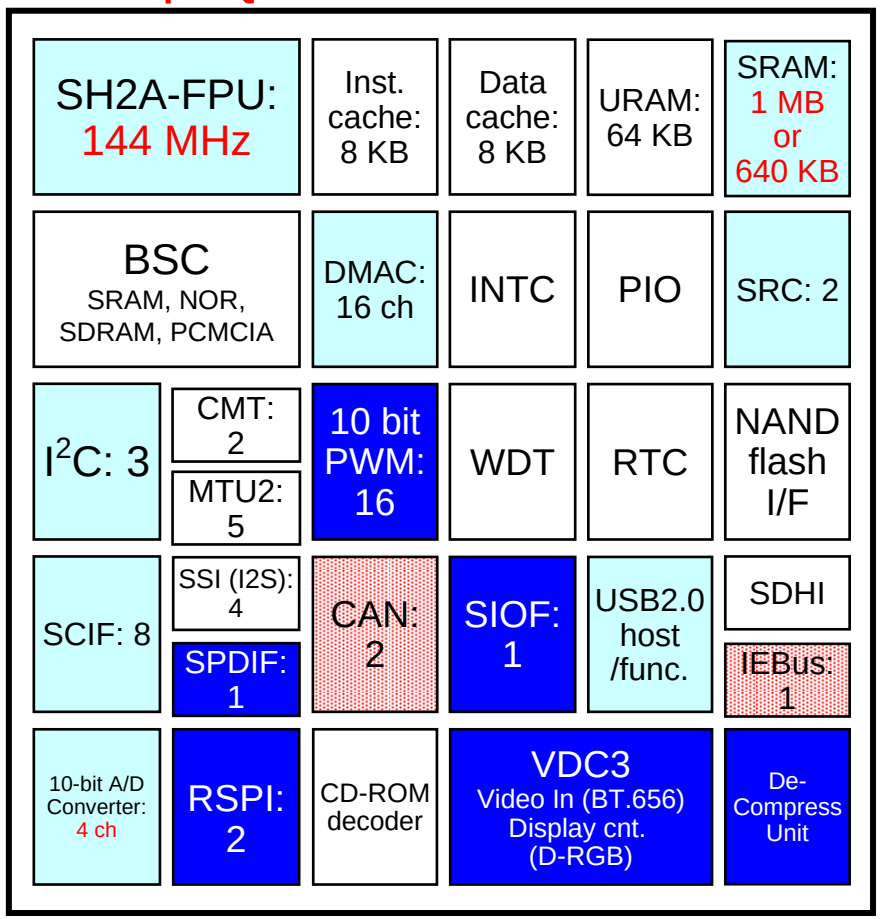
- **On-chip large-capacity SRAM (1 MB/640 KB)**
  - Reducing requirements for external SDRAM facilitates reducing numbers of parts and system costs.
  - For display sizes up to WQVGA, the SRAM is capable of holding dual frame buffers.
  - External SDRAM is still connectable.
- **USB2.0 and graphics functions**
  - Products incorporate a USB controller for High-Speed USB2.0 and a display controller that handles video input.
- **Abundant peripheral functions**
  - Inclusion of on-chip peripheral functions such as the FPU, CAN, MTU2, and PWM timers for motor control makes the products suitable for industrial applications.
  - Flash memory (NOR, NAND, serial flash memory etc.) is connectable.

Outline of the SH7262 Specifications

Under Development

SH7262

- CPU: SH2A-FPU (SuperH RISC engine)
- Frequency: CPU 144 MHz/External bus 72 MHz (max.)
- Power: Internal 1.2 V/External 3.3 V
- Internal Memory
  - URAM: 64 KB
  - SRAM: 1 MB (includes standby RAM: 32 KB)
    640 KB (includes standby RAM: 320 KB)
  - Cache: Instruction = 8 KB, data = 8 KB
- External memory interface
  - SRAM, NOR-type flash memory, SDRAM, PCMCIA
  - Bus width: 8 or 16 bits, memory space: 64 MB (max.)
- Peripheral modules
  - DMAC: 16 ch
  - USB host/function: 1
  - Multi function timer (MTU2): 5
  - 16-bit timer (CMT): 2
  - 10-bit PWM timer: 16
  - Watchdog timer (WDT): 1
  - Real-time clock (RTC): 1
  - I^2C bus interface: 3
  - Serial communication interface with FIFO (SCIF): 8
  - Renesas serial peripheral interface (RSPI): 2
  - Clock synchronous serial interface with FIFO (SIOF): 1
  - RCAN: 2 (option)
  - Video display controller (VDC3):
    D-RGB (up to WQVGA)
    Video IN (BT. 656)
  - NAND-type flash memory controller
  - Serial sound interface (SSI): 4
  - SPDIF: 1
  - Sample rate converter (SRC): 2
  - CD-ROM decoder
  - **10 bit A/D converter: 4 ch**
  - Decompression unit
- Peripheral modules
  - SD card host interface (SDHI): 1
  - IEBus: 1 (option)
- Package
  - **176-pin QFP**



Functionality added to that of the current product (SH7263)

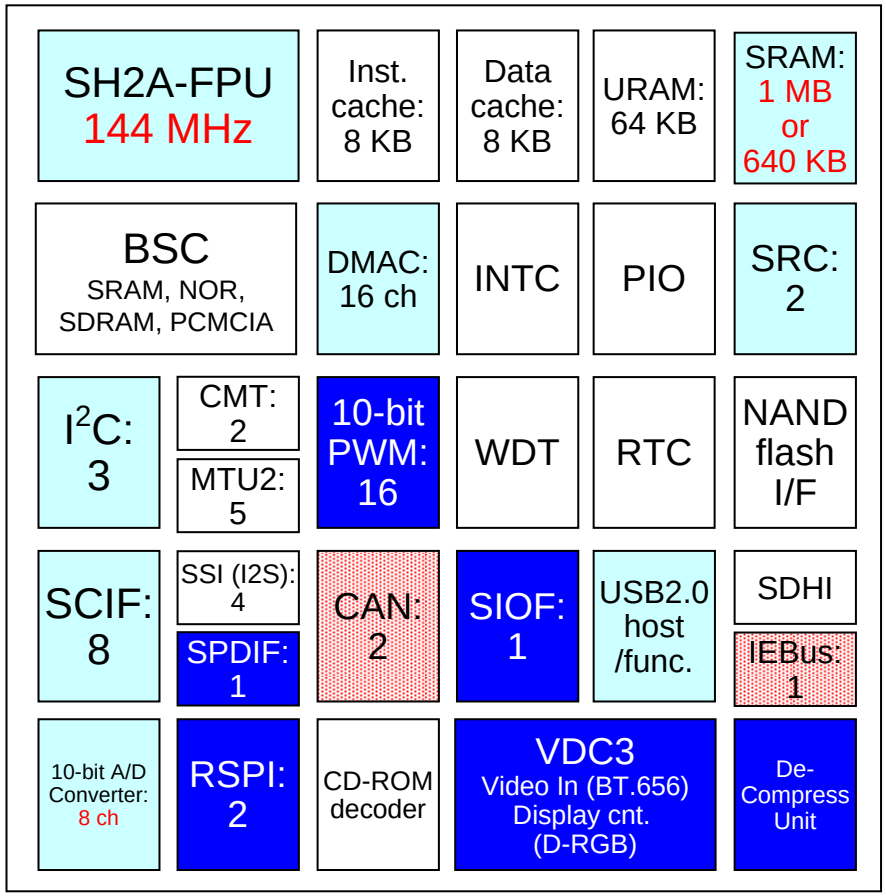
Option

Outline of the SH7264 Specifications

Under Development

SH7264

- CPU: SH2A-FPU (SuperH RISC engine)
- Frequency: CPU 144 MHz/external bus 72 MHz (max.)
- Power: Internal 1.2 V/external 3.3 V
- Internal Memory
  - URAM: 64 KB
  - SRAM: 1 MB (includes standby RAM: 32 KB)
    640 KB (includes standby RAM: 320 KB)
  - Cache: Instruction = 8 KB, data = 8 KB
- External memory interface
  - SRAM, NOR-type flash memory, SDRAM, PCMCIA
  - Bus width: 8 or 16 bits, memory space: 64 MB (max.)
- Peripheral modules
  - DMAC: 16 ch
  - USB host/function: 1
  - Multi-function timer (MTU2): 5
  - 16-bit timer (CMT): 2
  - 10-bit PWM timer: 16
  - Watchdog timer (WDT): 1
  - Real-time clock (RTC): 1
  - I^2C bus interface: 3
  - Serial communication interface with FIFO (SCIF): 8
  - Renesas serial peripheral interface (RSPI): 2
  - Clock synchronous serial interface with FIFO (SIOF): 1
  - RCAN: 2 (option)
  - Video display controller (VDC3):
    D-RGB (up to WQVGA)
    Video IN (BT. 656)
  - NAND-type flash memory controller
  - Serial sound interface (SSI): 4
  - SPDIF: 1
  - Sample rate converter (SRC): 2
  - CD-ROM decoder
  - **10-bit A/D converter: 8 ch**
  - Decompression unit
- Peripheral modules
  - SD card host interface (SDHI): 1
  - IEBus: 1 (option)
- Package
  - **208-pin QFP**



Functionality added to that of the current product (SH7263)

Option

Fields of Application

SH7262/SH7264

- **Digital audio devices**

  In-vehicle devices with USB, mini-and micro-component audio systems, iPod* accessories, etc.

- **Graphical dashboards**

  In-vehicle information panels, displays on AV centers, etc.

- **Office automation and industrial equipment**

  Copying machines, printers,etc.

  AC servomotors, general-purpose inverters, robots, sequencers,etc.

*: iPod is a trademark of Apple Inc., registered in the U.S. and other countries.

Development Concepts of SH7080 Series

Various features to achieve high-end embedded systems

Usage : Printers, DVD recorders, fax machines, AC servo motors, and inverters for industrial use.

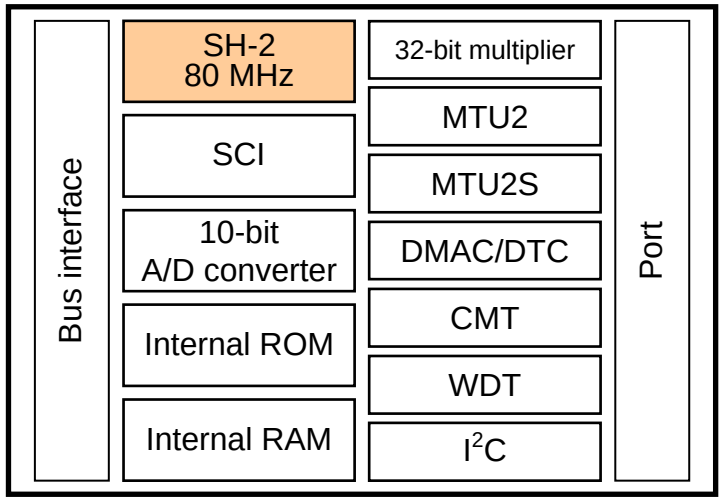
Feature 1	With on-chip high-speed flash memory and 80-MHz/104-MIPS high-performance CPU arithmetic operation	**Achieves high-performance control**
Feature 2	Upper model of SH7040/7144 Series and 3.3-V or 5-V single-power supply	**No need of external regulators**
Feature 3	Bus extension function and improved PWM timer, high-speed A/D converter (2.5 μs/ch)*1	**Peripheral functions suitable for machine and system controls**
Feature 4	On-chip debugging function, full spec. ICE, and JTAG-ICE are available.	**Reasonable development tools**

*1: $P\phi$ = 20 MHz

Overview of the SH7080

- CPU core
  - SH-2 (SuperH RISC engine)
  - 32-bit multiplier (32 bits × 32 bits → 64 bits)
- Operating Frequency
  - CPU clock: 80 MHz (max.)
  - External bus clock: 40 MHz (max.)
  - Peripheral clock: 40 MHz (max.)
  - Clock dedicated for MTU2S: 80 MHz (max.)
- Power Supply
  - 3.3 ±0.3 V or 5.0 ±0.5 V (5.0 ±0.5 V for analog supply)
- Internal Memory [ROM/RAM]
  - Flash version [512 KB/32 KB]: SH7083/84/85/86,
    [256 KB/16 KB]: SH7083/84/85
  - Mask version [256 KB/16 KB]: SH7083/84/85
  - ROM less version [RAM: 16 KB]: SH7083/84/85
- External Memory Interface
  - SRAM, SRAM with byte selection, multiplex I/O
  - SDRAM, PCMCIA, burst ROM *1
- Internal Functions
  - Multi-function 16-bit PWM timer: 6 (MTU2), 3 (MTU2S)
  - Port output enable (POE)
  - 16-bit cyclic timer: 2
  - Watchdog timer: 1
  - I^2C bus interface: 1*2
  - Synchronous serial interface unit: 1
  - DMA controller: 4 ch
  - DTC (simple DMA controller)
  - High-speed 10-bit A/D converter:
    4 ch × 2 (SH7083/84/85)
    4 ch × 2 + 8 ch (SH7086)
  - SCI: 4 (1 ch for 16-stage transmit and receive FIFO)

- Internal Functions
  - I/O port: 73 (SH7083), 84 (SH7084),
    108 (SH7085), 134 (SH7086)
  - External interrupt pins (NMI+IRQ): 9
  - On-Chip Debugging function (H-UDI)
- Packages
  - SH7083 (100-pin):
    TQFP1414-100 (14 mm square, 0.5-mm pitch)
  - SH7083 (BGA):
    P-LFBGA1010-112 (112 pin, 10 mm square)
  - SH7084 (112-pin):
    LQFP2020-112 (20 mm square, 0.65-mm pitch)
  - SH7085 (144-pin)
    LQFP2020-144 (20 mm square, 0.5-mm pitch)
  - SH7086 (176-pin)
    LQFP2424-176 (24 mm square, 0.5-mm pitch)



*1: Supported only at 3.3-V operation, and not supported at 5.0-V operation.
*2: SH7083 is not supported.

Development Concepts of SH7146 Series

Various features suitable for high-performance motor control.

Usage : Invertors for consumer electronics such as air-conditioning outside equipment and washing machine, invertors for general use, and devices for industrial use.

Feature 1	With on-chip high-speed flash memory and 80-MHz and 104-MIPS high-performance CPU arithmetic operation
Feature 2	Enhanced usability by 5-V single power supply
Feature 3	Improved two-way PWM timers Three high-speed A/D converters (2.5 μs/ch)*1
Feature 4	On-chip debugging functions: Full spec. ICE and JTAG-ICE

Achieves vector and PAM controls in a single chip

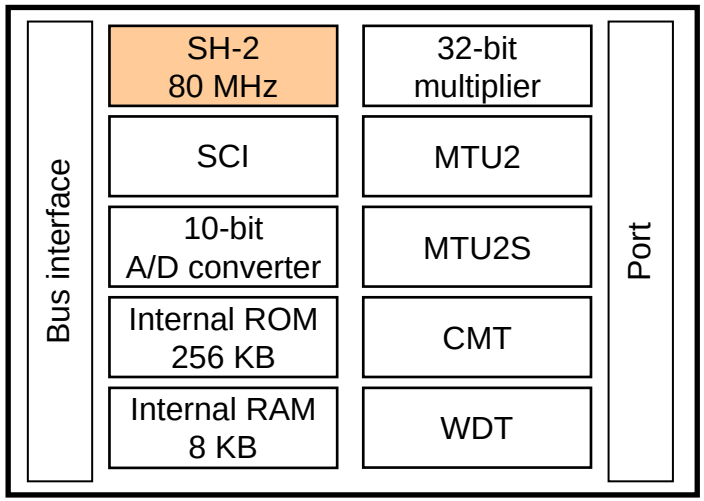
Realizes one-shunt vector control. Controls fan motor and compressor in a single chip

Reasonable development tools

*1: $P\phi = 20$ MHz

SH7146 Series Overview

- CPU core
  - SH-2 (SuperH RISC engine)
  - 32-bit multiplier
    (32 bits × 32 bits → 64 bits)
- Operating Frequency
  - CPU clock: 80 MHz (max.)
  - Bus clock: 40 MHz (max.)
  - Peripheral clock: 40 MHz (max.)
  - Clock dedicated for MTU2S: 80 MHz (max.)
- Power Supply Voltage
  - 4.0- to 5.5-V single power supply
- Internal Memory [ROM/RAM]
  - Flash version [256 KB/8 KB]: SH7146/SH7149
  - Mask version [256 KB/8 KB]: SH7146/SH7149
- External Memory Interface*1
  - 8-/16-bit external bus, SRAM I/F
- Internal Functions
  - Multi-functional 16-bit PWM timer:
    6 (MTU2), 3 (MTU2S)
  - Port output enable (POE): 9
  - Watchdog timer: 1
  - High-speed 10-bit A/D converter:
    2 ch × 2 + 8 ch (A total 12 ch)
  - DTC (simple DMA controller)*2
  - SCI: 3
  - I/O ports: 57 (SH7146), 75 (SH7149)
- Internal Functions
  - External interrupt pins (NMI+IRQ): 5
  - On-Chip Debugging function (H-UDI)*2
  - AUD function: Available only in the flash-memory version (SH7149) supporting full functions of the E10A for evaluation.
- Packages
  - SH7146 (80-pin):
    LQFP80 (14 mm square, 0.65-mm pitch)
  - SH7149 (100-pin):
    LQFP100 (14 mm square, 0.5-mm pitch)



*1: For external memory Interface, only SH7149 is supported. SH7146 is not supported.
*2: Not available in Mask-ROM versions.

Development Concept of SH7125 Series

Various features to realize small high-performance motor control system.

Usage : Invertors for consumer electronics such as refrigerators and vacuum cleaners, and motor control devices such as pumps, fans, and compressors.

Feature 1	32-bit RISC-engine microcomputer in a small package: 64 pins/48 pins
Feature 2	50-MHz and 65-MIPS high-performance CPU arithmetic operation
Feature 3	Improved PWM timers: Two high-speed A/D converters (2 μs/ch)
Feature 4	On-chip debugging functions: Full spec. ICE and JTAG-ICE

Much higher-performance of CPU compared to that of 8-bit/16-bit CPU

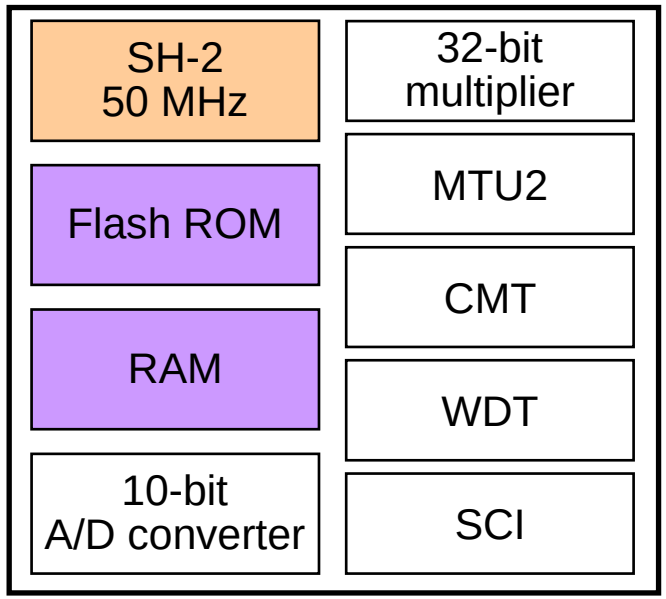
Achieves one-shunt vector control

Reasonable development tools

SH7125 Series Overview

- CPU core
  - SH-2 (SuperH RISC engine)
  - 32-bit multiplier
    (32 bits × 32 bits → 64 bits)
- Operating Frequency
  - CPU clock and peripheral I/O clock:
    50 MHz, 25 MHz or 40 MHz, 40 MHz
- Power Supply Voltage
  - 4.0- to 5.5-V single power supply
- Internal Memory (flash memory, RAM)
  - Flash memory: 128 KB/64 KB/32 KB/16 KB
  - RAM: 8 KB/4 KB
- Internal Functions
  - Multi-functional 16-bit PWM timer: 6 (MTU2)
  - Port output enable (POE)
  - Watchdog timer: 1
  - High-speed 10-bit A/D converter: 4 ch × 2 (total 8 ch)
  - SCI: 3
  - I/O ports: 33 (SH7125), 26 (SH7124)
  - External interrupt pins (NMI + IRQ):
    4 (SH7124), 5 (SH7125)
  - On-Chip Debugging function (H-UDI)*

- Packages
  - SH7125 (64-pin):
    LQFP-64 (10 mm square/0.5-mm pitch),
    QFP-64A (14 mm square/0.8-mm pitch),
    VQFN-64 (8 mm square/0.4-mm pitch)
  - SH7124 (48-pin):
    LQFP-48 (10 mm square/0.65-mm pitch)
    VQFN-52 (7 mm square/0.4-mm pitch)



Note *: The function is not included
in the 32- and 16-KB ROM versions.

Development Concepts of SH7147 Series

Various features suitable for high-performance motor control.

Usage: Power steering systems, hybrid electric vehicles, general-purpose inverters, inverter control of AC servo, etc.

Feature 1	80-MHz and 104-MIPS high-performance CPU arithmetic operation
Feature 2	Single-cycle access to high-speed flash memory at 80 MHz
Feature 3	Peripheral functionality dedicated for motor control • A 12-bit resolution A/D converter enables simultaneous sampling of all phases of a three-phase motor. • Timers for a three-phase motor (Multi-function timer pulse unit 2 and Multi-function timer pulse unit 2S)
Feature 4	Abundant communications interface functions (RCAN-ET, Synchronous Serial Communication Unit, Serial Communication Interface)

Achieves vector control of a motor

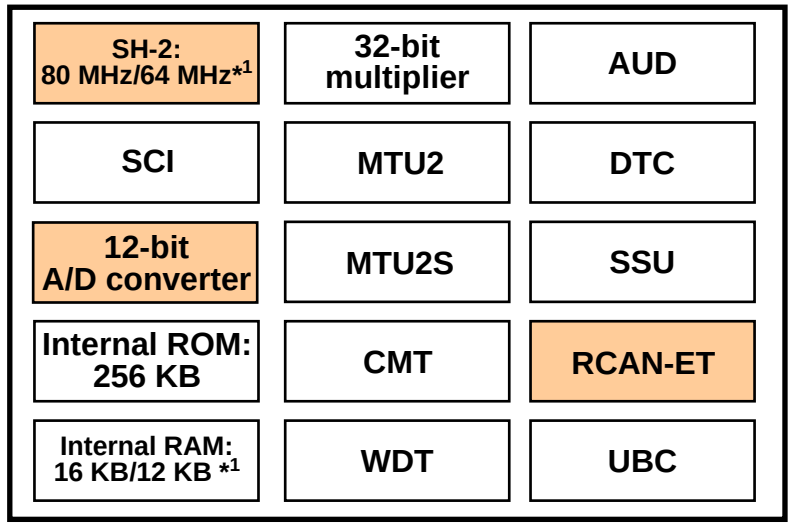
A single chip can control two three-phase brushless motors.

Overview of SH7147 Series

- CPU core
  - SH-2 (SuperH RISC engine)
  - 32-bit multiplier (32 bits × 32 bits → 64 bits)
- Operating Frequency
  - CPU clock: 80 MHz (max.) /64 MHz (max.) *1
  - Bus clock: 40 MHz (max.) /32 MHz (max.) *1
  - Peripheral clock: 40 MHz (max.) /32 MHz (max.) *1
  - Clock dedicated for Multi-function timer pulse unit 2S: 80 MHz (max.) /64 MHz (max.) *1
- Power-Supply Voltage
  - 80-MHz/5.0-V single power supply
  - 64 MHz/3.3 V (internal), 5.0 V (I/O, analog power supply) *1
- Internal Memory
  - Flash memory: 256 KB/384 KB/512 KB
  - Internal RAM: 16 KB/12 KB
- External Memory Interface
  - 8-bit external bus, SRAM interface
- Internal Functions
  - 16-bit multifunctional PWM timer: 5 (Multi-function timer pulse unit 2), 3 (Multi-function timer pulse unit 2S)
  - Port output enable (POE)
  - Advanced user debugger (RAM-monitoring function)
  - Data transfer controller (simplified DMA controller)
  - Synchronous serial interface unit (SSU): 1
  - Serial communications interface: 3
- Internal Functions
  - High-speed, 12-bit A/D converter: 8 ch × 2 (total 16 ch)
  - Controller Area Network (RCAN-ET)
  - Watchdog timer: 1
  - I/O ports: 57
  - External interrupt pins (including NMI): 5
- Package
  - LQFP1414-100 (14-mm square, 0.5-mm pitch)

Target Applications

- Automobile field: power steering systems, inverter control of hybrid electric vehicles
- Industrial field: general-purpose inverters, AC servo motors



Note) *1: temperature range (-40 to 125 ˚C)

Development Concepts of the SH7137

Various features to adapt to high-performance motor control system

Applications: Inverters, AC servo motors, manipulators, measuring equipment, etc. for industrial use

Feature 1:	High-performance CPU arithmetic operation at 80 MHz/104 MIPS
Feature 2:	Single-cycle access to high-speed flash memory at 80 MHz
Feature 3:	On-chip peripheral functional modules dedicated for motor control • A 12-bit resolution A/D converter enables simultaneous sampling of all phases of a three-phase motor. • On-chip timer for a three-phase motor (MTU2 and MTU2S)
Feature 4:	Abundant communications interface functions (RCAN-ET, SSU, SCI)
Feature 5:	On-chip debugging functions Full ICE and JTAG-ICE are available.

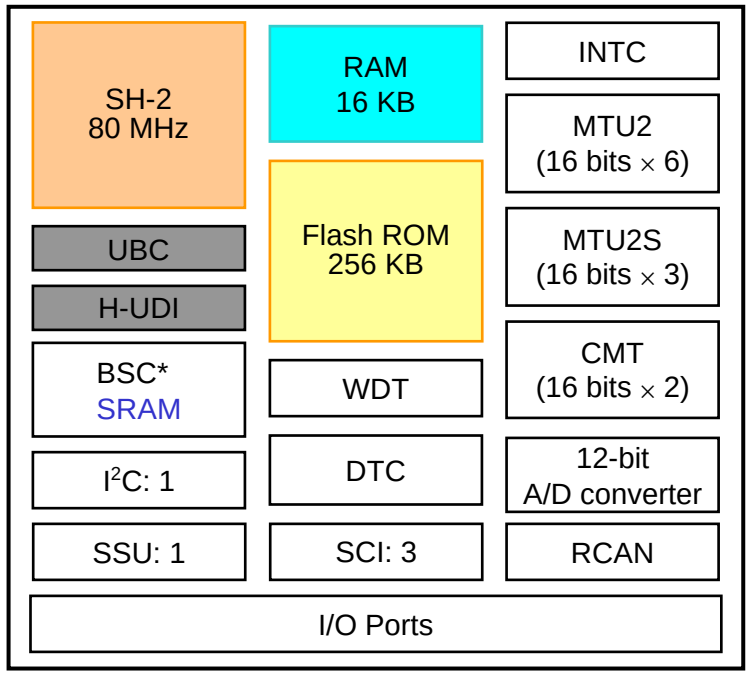
Vector control of a motor is enabled.

A single chip can control two 3-phase brushless motors.

Reasonable development tool

Functional Outline of the SH7137

- CPU core
  - SH-2: SuperH RISC engine
- Operating frequency
  - CPU clock: 80 MHz (max.)
  - Bus clock: 40 MHz (max.)
  - Peripheral clock: 40 MHz (max.)
- Power-supply voltage
  - 3.3 V±0.3 V or 5.0 V±0.5 V
    Single-power supply (AVcc = 5.0 V±0.5 V)
- On-chip memory
  - 256-KB Flash memory
  - 16-KB RAM
- External memory interface
  - SH7136: None
  - SH7137: External bus width is 8 bits.
- Internal peripheral function
  - Multi-functional 16-bit PWM timer: 6 (MTU2), 3 (MTU2S)
  - Port output enable (POE)
  - Compare match timer (CMT): 2
  - Watchdog timer (WDT): 1
  - Data transfer controller (DTC)
  - Serial communications interface (SCI): 3
  - Synchronous communications interface (SSU): 1
  - I^2C bus interface: 1
  - RCAN-ET: 1
  - A/D converter:
    12 bits × 16 ch (SH7137), 12 bits × 12 ch (SH7136)
- On-chip debugging function
  - H-UDI
  - User break controller (UBC)
- Packages
  - SH7136: LQFP1414-80
    (14-mm square, 0.65-mm pitch)
  - SH7137: LQFP1414-100
    (14-mm square, 0.5-mm pitch)



Note *: Only available for SH7137

SH7144 Series Overview

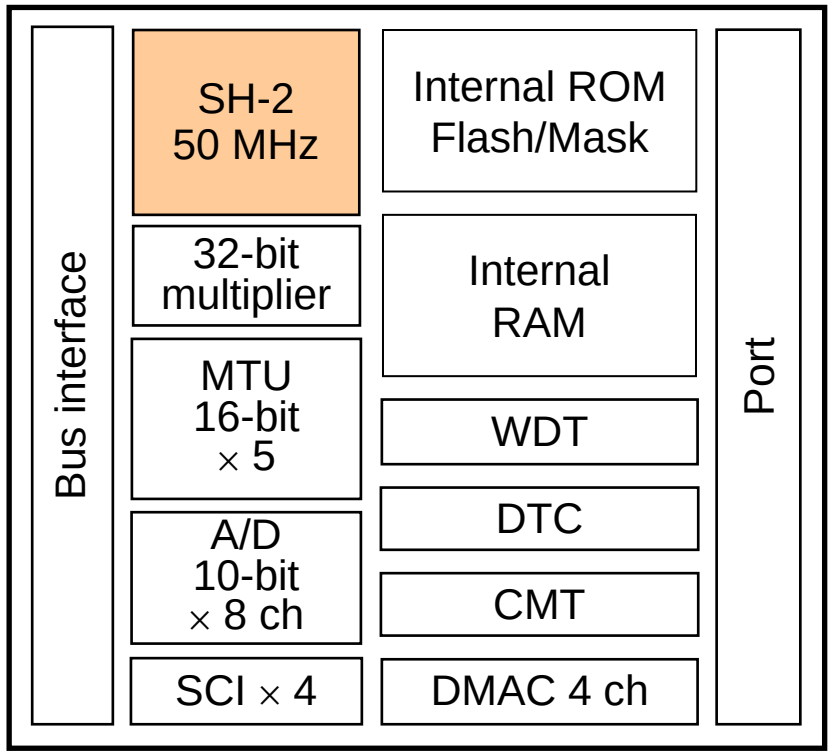
Features

- CPU core
  - SH-2 with an operating frequency of 50 MHz, 3.0 to 3.6 V operation
  - 32-bit multiplier (32 bits × 32 bits → 64 bits)
- Internal memory
  - ROM: 256 KB (Flash/Mask/ROMless)
  - RAM: 8 KB
- Internal functions
  - Multi-functional 16-bit timer (MTU): 5
  - Internal DMAC and DTC
  - External bus: 8/16/32 bits
  - A/D converter: 10 bits, 8 ch (4 ch × 2 units)
  - SCI: 4
  - I^2C: 1
- Package
  - QFP-112 (SH7144)/LQFP-144 (SH7145)

Main areas of application

- Digital consumer appliances, OA equipment industrial use

SH7144 Series Block Diagram



SH7046 Overview

- Single-Chip Microcomputer in a Small Package -

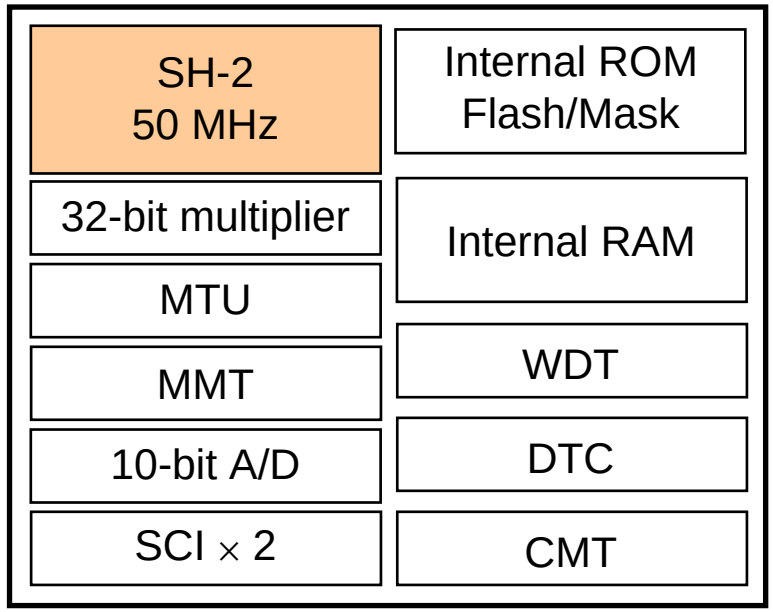
Features

- CPU core
  - SH-2 (Renesas's original SuperH 32-bit RISC)
  - Max. operating frequency: 50 MHz @ 4.0- to 5.5-V operation
  - 32-bit multiplier (32 bits × 32 bits → 64 bits)
  (The SH7101: 40 MHz)
- Internal functions
  - Powerful 16-bit timer (MTU, MMT)
  - Enables output of a max. 15-phase PWM waveform
  - Built-in DTC
  - A/D converter: 10 bits, 12 ch (4 ch × 3 units)
  - SCI: 2
  (SH7101: Without MMT and DTC 8 channel A/D converter (4 ch × 2 units))

Main applications

- White ware goods with inverters such as air conditioners, washing machines, and refrigerators, and industrial applications such as inverters, AC servos, FA, UPS, and FA sequencers

SH7046 Block Diagram



80-pin QFP

	ROM	RAM
SH7046F (Flash Version)	256 KB	12 KB
SH7104 (Mask Version)*	256 KB	8 KB
SH7048 (Mask Version)	128 KB	4 KB
SH7108 (Mask Version)*	128 KB	4 KB
SH7148 (Mask Version)	64 KB	4 KB
SH7106 (Mask Version)*	64 KB	4 KB
SH7101 (Mask Version)**	32 KB	2 KB

*: Without DTC **: Without DTC and MMT

SH7047 Overview

- Microcomputer with a Built-in CAN Bus Interface -

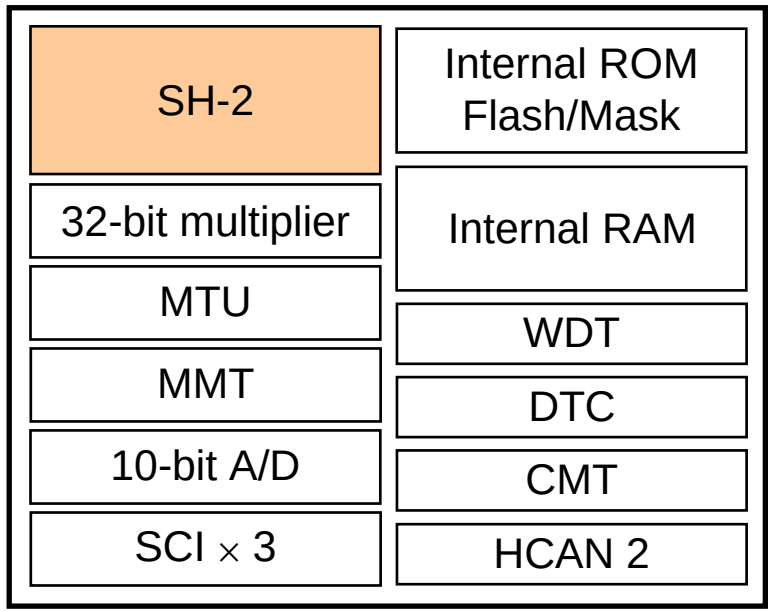
Features

- CPU core
  - SH-2 (Renesas original SuperH 32-bit RISC)
  - Max. operating frequency: 50 to 40 MHz @ 4.5 to 5.5-V operation
  - 32-bit multiplier (32 bits × 32 bits → 64 bits)
- Internal functions
  - Powerful 16-bit timer (MTU, MMT)
  - Enables output of a max. 15-phase PWM waveform
  - Built-in DTC
  - A/D converter: 10 bits, 16 ch (8 ch × 2 units)
  - SCI: 3
  - HCAN2: 1

Main applications

- Automobile applications such as EPS and airbags, and industrial applications such as inverters, AC servo, FA, UPS, and FA sequencers

SH7047 Block Diagram



100-pin QFP

	ROM	RAM
SH7047F (Flash Version)	256 KB	12 KB
SH7049 (Mask Version)	128 KB	8 KB
SH7105 (Mask Version)*	256 KB	8 KB
SH7109 (Mask Version)*	128 KB	4 KB
SH7107 (Mask Version)*	64 KB	4 KB

* SCI: 2, Without DTC

SH7040 Series Overview

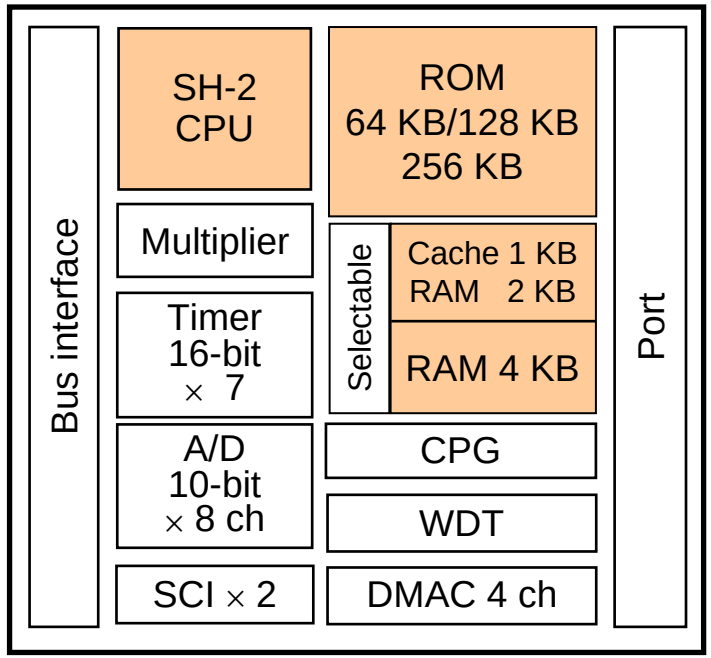
Features

- SH-2 core high-performance single-chip RISC
  - 37 MIPS/28.7 MHz
  - Built-in 32-bit multiplier
- Built-in large-capacity memory
  - ROM: 64 KB (mask)/128 KB (mask, OTP)/ 256 KB (mask, Flash)/ROMless
  - RAM: 4 KB (can be used as 1-KB cache + 2-KB RAM)
- Built-in cache memory
  - 1-KB instruction cache, 256 entries, and direct mapping
- Various peripheral functions
  - Powerful timer: MTU, 2-ch compare-match timer
  - A/D converter: 10 bits × 8 ch
  - Serial interface: 2
  - DMAC: 4 ch
- Products lineup (ROMless type is also available)

	ROM size	Package
SH7040/42/44	64 KB/128 KB/256 KB	QFP-112
SH7041/43/45	64 KB/128 KB/256 KB	QFP-144

Note: SH7042 (3.3-V Version): TQFP-120

SH7040 Series Block Diagram



Main applications

- Motor controls, navigation systems, digital cameras, PPCs, printers, faxes, and JPEG application system

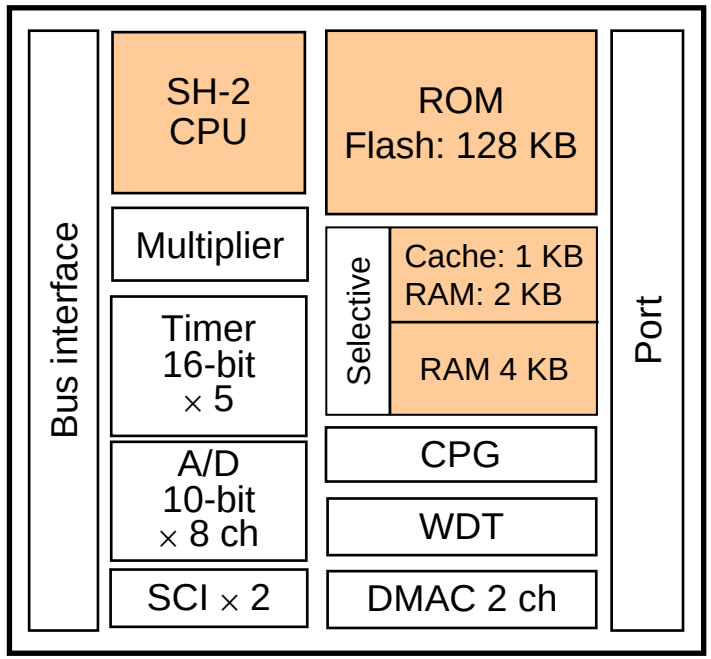
SH7014, SH7016, and SH7017 Overview

Features

- High-performance single-chip RISC with SH-2 core
  - 37 MIPS/28.7 MHz/5 V
  - Built-in 32-bit multiplier
- Built-in memory
  - ROM: 64 KB (Mask)/128 KB (Flash)/ROMless
  - RAM: 3 KB/4 KB
    (can be used as 1-KB cache + 1-KB/2-KB RAM)
- Built-in cache memory
  - 1-KB instruction cache, 256 entries, and direct mapping
- Peripheral functions
  - Powerful timer: 16 bits × 5 (MTU: 0-2, CMT: 2)
  - A/D* converter: 10 bits × 8 ch
  - Serial interface: 2
  - DMAC: 2 ch
- Product lineup

	ROM size	RAM	Package	f/V
SH7014	-	3 KB	QFP-112	
SH7016	64 KB (Mask)	3 KB	QFP-112	28.7 MHz/5 V
SH7017	128 KB (Flash)	4 KB	QFP-112	

SH7017F Block Diagram



Main applications

- Video printers, liquid crystal projectors, Scanners, and electronic musical instruments, etc.

*: A/D module is different between SH7014 and SH7016/17

SH7020 and SH7030 Series Overview

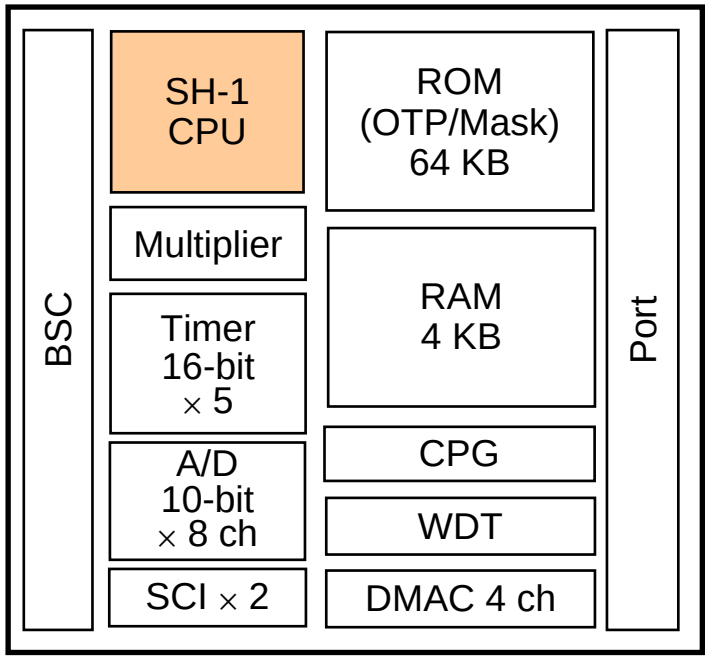
- Another Low Price ROMless Version is Added to the Lineup -

Features

- 32-bit single-chip RISC with high-performance
  - 26 MIPS/20 MHz
- Built-in 16-bit multiplier
- Various built-in large-capacity memories
  - ROM: 64 KB/32 KB/16 KB/ROMless
  - RAM: 8 KB/4 KB/1 KB
- Various built-in peripheral functions
  - 16-bit timer, A/D converter, DMAC, SCI, INTC, Bus state controller (BSC), etc
- Package
  - TQFP-120, QFP-112, and TQFP-100
- Product lineup
  - 5 types (ROMless Versions for the SH7034 and SH7020 also available)

	ROM/RAM	A/D	Package
SH7032	-/8 KB	Yes	QFP-112 TQFP-120
SH7034	64 KB/4 KB	Yes	
SH7034B	-/4 KB	Yes	
SH7021	32 KB/1 KB	-	TQFP-100
SH7020	16 KB/1 KB	-	

SH7034 Block Diagram



Main applications

- Motor controls, FAs, navigation systems, HDDs, printers, faxes, digital cameras, etc

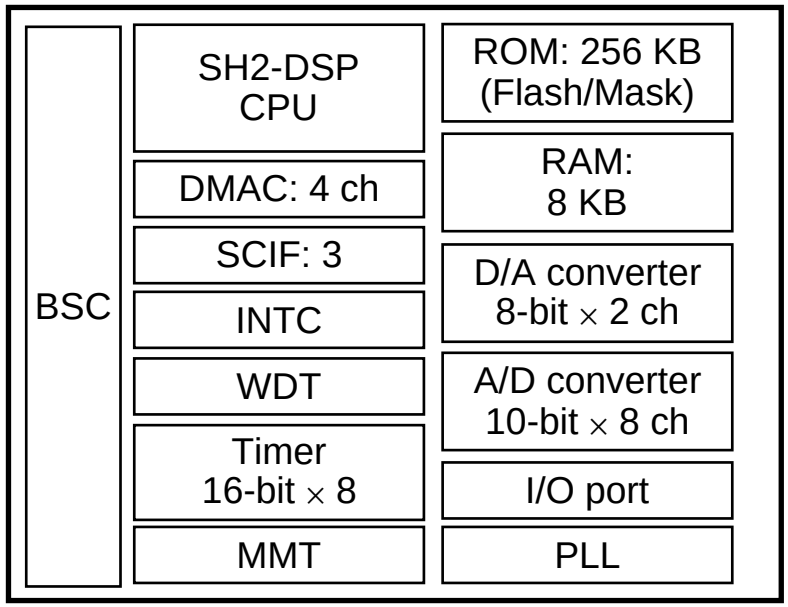
SH7065 Overview

- High-Performance Single-Chip RISC Microcomputer with a Built-in Large-Capacity Flash Memory -

Features

- SH-core (with an enhanced DSP function) high-performance single-chip RISC
  - 60 MHz/3.3 V
  - All SH-2 instructions + DSP-function enhanced instructions (SH2-DSP core)
- Built-in large-capacity memory
  - ROM: 256 KB (Flash/Mask)
  - RAM: 8 KB (X-RAM: 4 KB, Y-RAM: 4 KB)
- Powerful peripheral functions
  - Timers: TPU (6) + CMT (2) + MMT (1)
  - A/D converter: 10 bits × 4 ch × 2 units
  - D/A converter: 8 bits × 2 ch
  - SCIF: (FIFO) 3
  - DMAC: 4 ch
  - INTC (interrupt controller), WDT etc
- Bus state controller (BSC)
  - Directly connected with ROM/SRAM/DRAM/EDO
- Power management unit
  - Can be switched between the CPU, internal peripheral, and external bus clock
  - Module standby function
- Endian switching of external data available
- Package
  - LQFP-176 (24 mm × 24 mm, 0.5-mm pitch)

SH7065 Block Diagram



Main applications

- MFPs, high-performance digital cameras, digital video cameras, DVD systems, communication terminals, and industrial controllers

SuperH with Built-in Ether

SH-Ether Overview

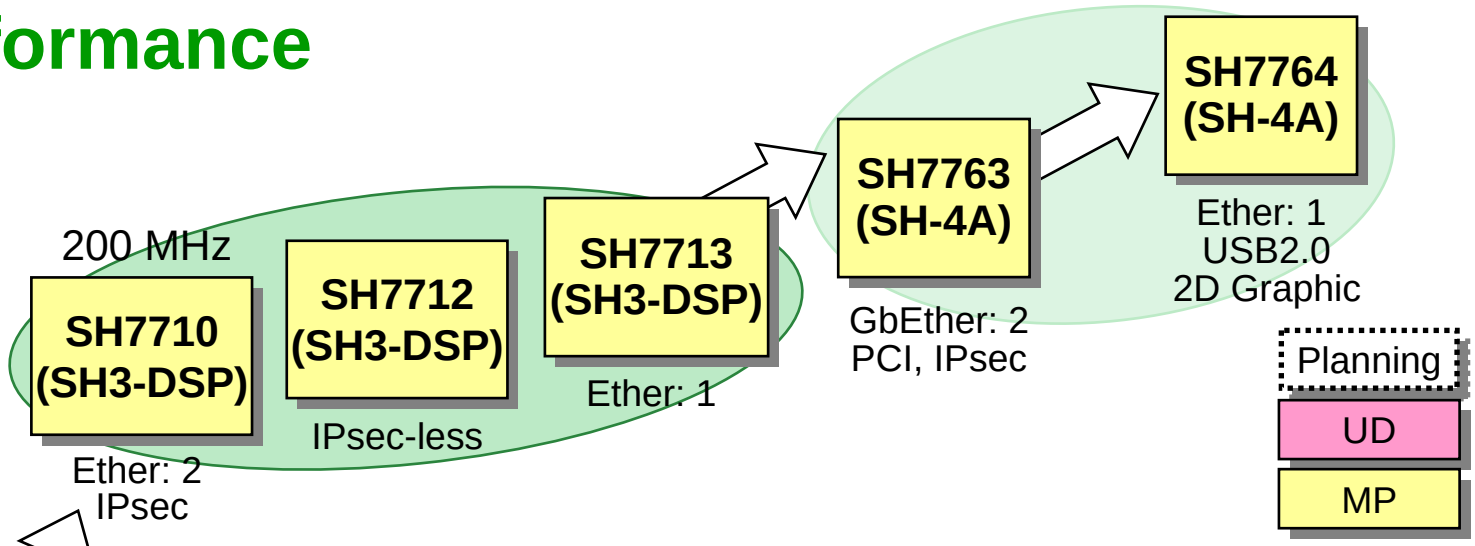
The SH-Ether Series products are the SuperH microcomputers equipped with the 10/100-Mbps supporting Ethernet controllers in compliance with the IEEE802.3u standard.

- Target applications
  - LBPs (Laser Beam Printer), MFPs (Multi Function Printer)
  - LAN cards (PC peripherals, FA devices)
  - Digital home electronics, IP Phones
  - Amusement devices
  - POS systems
  - Monitoring systems
  - Others
    (The Ethernet required systems)

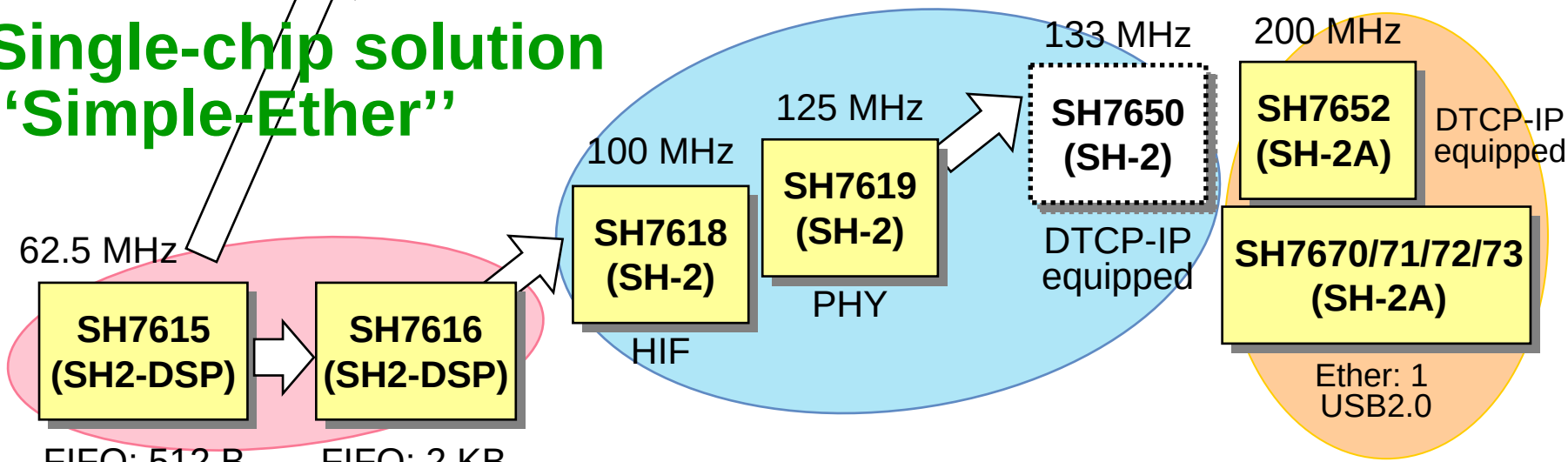
Adopted for various embedded Ethernet systems

SH-Ether Roadmap

High Performance SH-Ether



Single-chip solution "Simple-Ether"

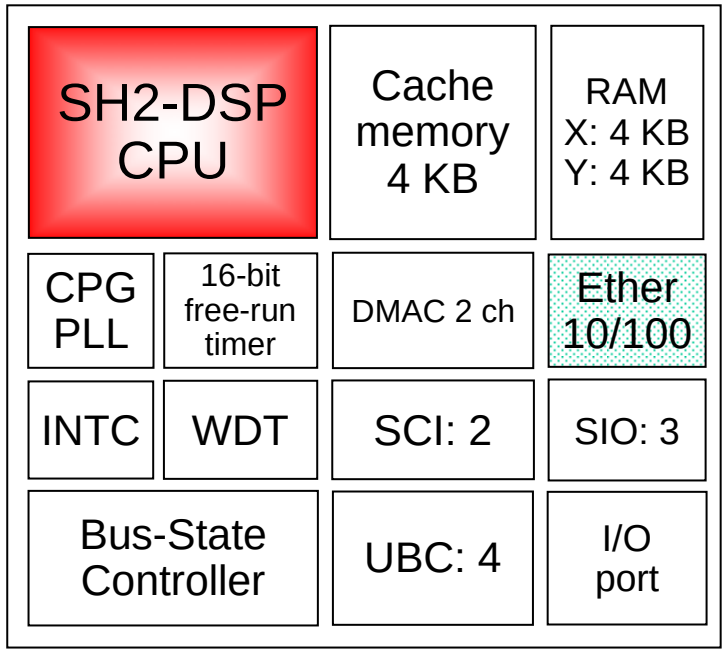


SH7615 Overview

Features

- High performance RISC engine SuperH core (SH2-DSP)
  - 81 MIPS, 125 MOPS (max.) @62.5 MHz
- Instruction/data combination type cache (4 KB)
  - 4-way set associative, 64 entries, 16-byte line length
- Internal RAM (8 KB)
- SDRAM Interface
  - Supports high-speed access: external bus to 62.5 MHz (max.)
  - Possible 16 Byte DMA dual burst access
- Ethernet controller (MAC*1: accordance with IEEE802.3u)
  - transmission rate: 10/100 Mbps, Full duplex transmit and receive
  - Assembles/Disassembles data frame, CRC
  - Supports MII*2, Magic packet ™*3
  - FIFO 512 Byte each for transmission and reception
- Boundary Scan
  - Boundary Scan Function (accordance with IEEE1149.1)
- Peripheral function
  - TPU (3), SCIF (2), DMAC (2), INTC, WDT (1), FRT (1), SIO (3), I/O port etc
- Vcc = 3.3 V (supports 5 V I/F regarding I/O and Ethernet pin)

SH7615 Block Diagram



Ether FIFO = 512 B
Package: QFP-208 / CSP-240

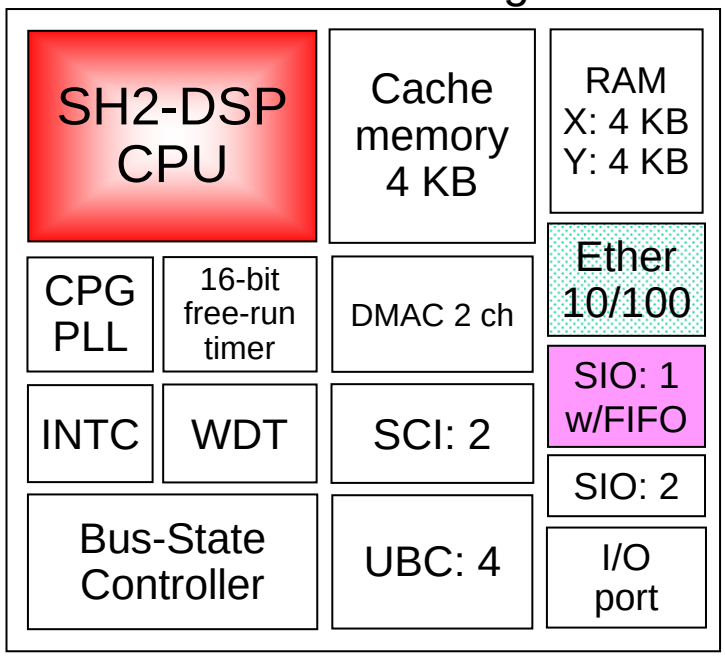
*1 MAC:Media Access Control,
*2 MII:Media Independence Interface,
*3 Magic Packet is a trademark of Advanced Micro Devices, Inc.

SH7616 Overview

Features

- High performance RISC engine SuperH core (SH2-DSP)
  - 81 MIPS, 125 MOPS (max.) @62.5 MHz
- Instruction/data combination type cache (4 KB)
  - 4-way set associative, 64 entries, 16-byte line length
- Internal RAM (8 KB)
- SDRAM Interface
  - Supports high-speed access: external bus to 62.5 MHz (max.)
  - Possible 16 Byte DMA dual burst access
- Ethernet controller (MAC[*1]: accordance with IEEE802.3u)
  - transmission rate: 10/100 Mbps, Full duplex transmit and receive
  - Assembles/Disassembles data frame, CRC
  - Supports MII[*2], Magic packet™[*3]
  - FIFO 2 KB each for transmission and reception
- Boundary Scan
  - Boundary Scan Function (accordance with IEEE1149.1)
- Peripheral function
  - TPU (3), SCIF (2), DMAC (2), INTC, WDT (1), FRT (1), SIO (2), I/O port etc
  - SIO with FIFO (16 bits × 16) for CODEC
- Vcc = 3.3 V (supports 5 V I/F regarding I/O and Ethernet pin)

SH7616 Block Diagram



Ether = 2 KB
SIO with FIFO 1 ch
Package: QFP-208

*1 MAC: Media Access Control,
*2 MII: Media Independence Interface,
*3 Magic Packet is a trademark of Advanced Micro Devices, Inc.

Difference Between SH7615 and SH7616

FIFO (up to 2 KB)

- Possible one transaction per frame
- Improve the efficiency of transmission and reception of frames

CAM match signal

- Multi Address support
- Useful for FA network

SIOF (SIO with FIFO)

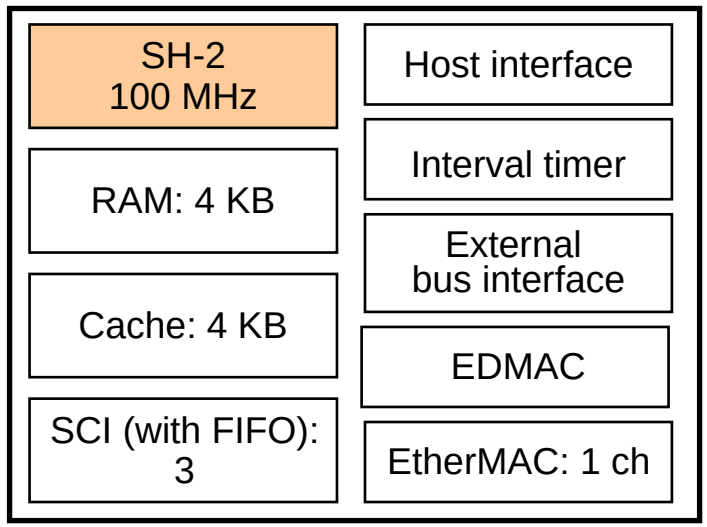
- Improve the efficiency of G.729a handling
- Support for CODEC having Communication Data
  e.g. Si 3000 (Silicon Laboratories), STLC7550 (SGS Thompson)

Overview of SH7618/7618A Specifications

- Inexpensive network controller incorporating EtherMAC and host interface -

- CPU core
  - SH-2 (SuperH 32-bit RISC engine, 32-bit multiplier)
  - PVcc = 3.0 to 3.6 V, Vcc = 1.4 to 1.6 V
- Operating Frequency
  - CPU clock: 100 MHz
  - Bus clock: 50 MHz
- Internal Memory
  - RAM: 4 KB
  - Cache memory:
    4 KB (Four-way set associative): 7618
    16 KB (Four-way set associative): 7618A
- Host I/F
  - 1 KB × 2 sections
  - HIF boot function
- Ethernet functions
  - EtherMAC (10/100 Mbps): 1 ch
  - MII is also available.
  - Transmit and receive FIFO: 256 bytes each (7618), 512 bytes each (7618A)
  - Dedicated DMA controller: 2 ch
- External Memory Interfaces
  - SRAM, SDRAM, and PCMCIA I/F
  - Switchable to big/little endian
  - External bus can be extended up to 16 bits

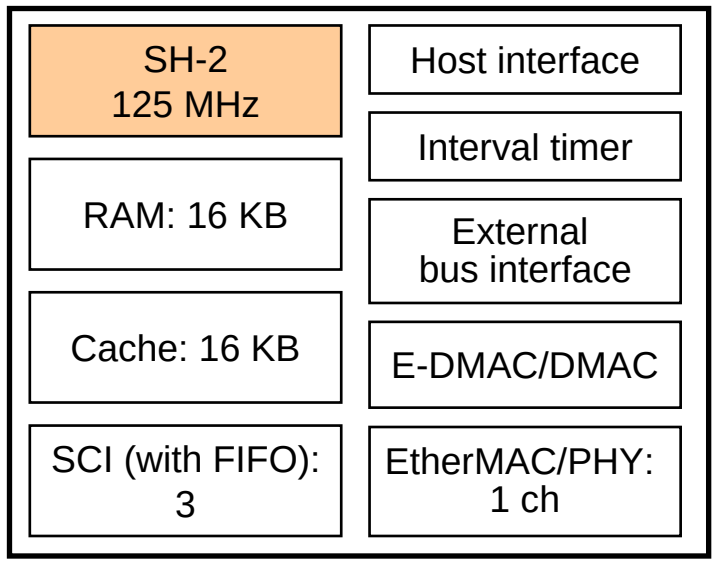
- Peripheral Functions
  - Serial communication interface: 3
    Switchable to UART/clock synchronous
    16-stage transmit and receive FIFO
  - 16-bit interval timer: 2
  - Watchdog timer: 1
  - General-purpose I/O port: 78
  - JTAG interface support
  - External interrupt pins: 9
- Package
  - CSP-176 (13 mm square, 0.8-mm pitch)



Overview of SH7619 Specifications

- PHY in a single chip improves performance -

- CPU core
  - SH-2 (32-bit SuperH RISC engine, 32-bit multiplier)
  - PVcc = 3.0 to 3.6 V, Vcc = 1.7 to 1.9 V
- Operating Frequency
  - CPU clock: 125 MHz
  - Bus clock: 62.5 MHz
- Internal Memory
  - RAM: 16 KB
  - Cache memory: 16 KB (4-way set associative)
- Host I/F
  - 1 KB × 2 sections
  - HIF boot function
- Ethernet Functions
  - EtherMAC (10/100 Mbps): 1 ch
  - EtherPHY (10/100 Mbps): 1 (MII is also available)
  - Transmit and receive FIFO: 512 bytes each
  - Dedicated DMA controller: 2 ch
- External Memory Interface
  - SRAM, SDRAM, and PCMCIA
  - Switchable to big/little endian
  - External bus can be extended up to 32 bits
- General-Purpose DMA Controller
  - 4 ch
- Peripheral Functions
  - Serial communication interface: 3
    Switchable to UART/clock synchronous
    16-stage transmit and receive FIFO
  - 16-bit interval timer: 2
  - Watchdog timer: 1
  - General-purpose I/O ports: 78
  - JTAG interface support
  - External interrupt pins: 9
- Package
  - CSP-176 (13 mm square, 0.8-mm pitch)



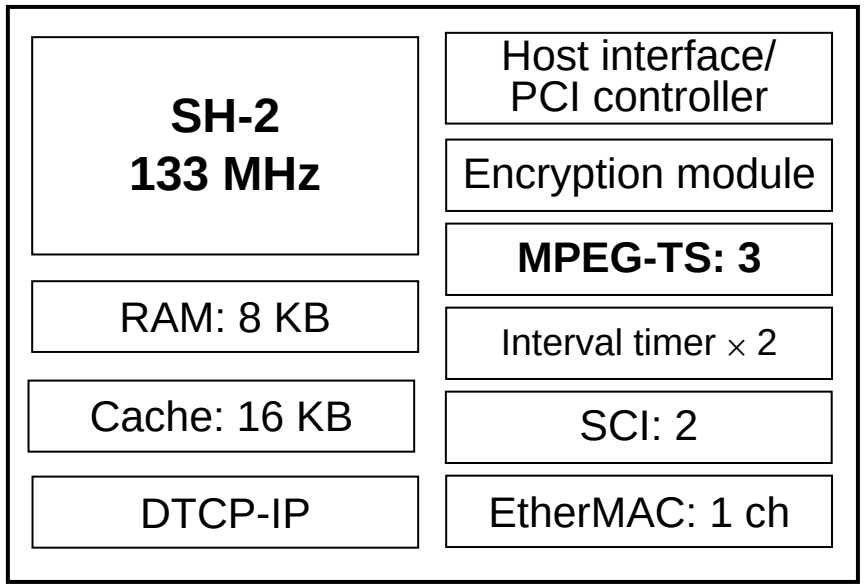
SH7650 Functions and Features

- Incorporates high-performance SH-2 core
  - Realizes network processing and DTCP processing at 173 MIPS@133 MHz with no load on the main CPU
- On-chip functions supporting DTCP-IP*
  - Authentification between systems and encryption/decryption of contents are achieved by hardware and supplied firmware
- Internal PCI bus controller and host interface
  - Facilitates connection with the main CPU
- Includes wireless LAN interface and MPEG-TS port for moving image streaming
- Abundant bus interfaces
  - SDRAM interface
  - Burst ROM interface, etc.

*: DTCP-IP standard is a standard for protecting contents on the IP network standardized by DTLA (Digital Transmission Licensing Administrator)

SH7650 Overview

- CPU core
  - SH-2
    (SuperH 32-bit RISC, with on-chip 32-bit multiplier)
  - PVcc = 3.0 to 3.6 V, Vcc = 1.4 to 1.6 V
- Operating frequency
  - CPU clock: 133 MHz
  - Bus clock: 66 MHz
- Internal memory
  - Internal RAM: 8 KB
  - Cache memory: 16 KB
- On-chip DTCP-IP
- Host interface
  - 1 KB × 2 banks
  - Includes HIF boot function
- PCI controller
  - 33 MHz/32 bits
- Ethernet controller
  - EtherMAC (10/100 Mbps): 1 ch
  - Includes MII
  - Transmit/receive FIFO: each 512 bytes
  - Dedicated DMA controller: 2 ch
  - Incorporates TCP/IP checksum accelerator
- Memory interface
  - SRAM, SDRAM interface
  - External bus can be extended up to 32 bits
- Encryption module
  - AES encryption/decryption
  - Dedicated DMA controller
- On-chip MPEG-TS interface
  - Includes 3 channels
- Peripheral functions
  - Serial communication interface: 2
  - 16-bit interval timer: 2
  - Support for JTAG interface, external interrupt pin, and I/O ports
- Package
  - CSP-336 (17-mm square, 0.8-mm pitch)



SH7652 Overview

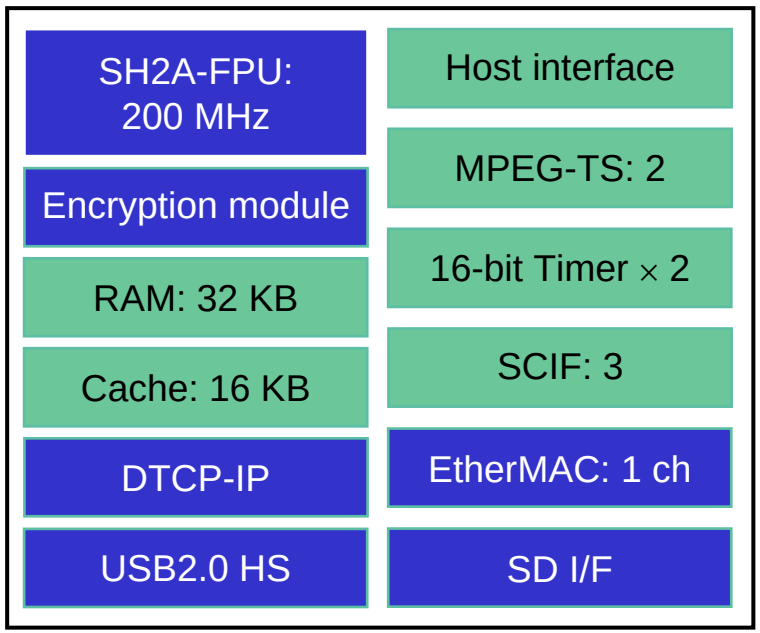
- Network processor with DTCP-IP function for DLNA (Digital Living Network Alliance) incorporated -

- Network-specialized cost performance
  - SH-2A core: 200 MHz
- DTCP-IP -support functions
  - An inter-device authentication function and content encryption/decryption function implemented by hardware and firmware provided with the SH7652, compliant with the DTCP-IP standard.
  - Network functions for IP broadcasting
- USB 2.0 High Speed and SD host interface
- Abundant bus interfaces
  - SDRAM I/F
  - Burst ROM I/F etc.

Functional Overview of SH7652

- CPU core
  - SH2A-FPU (32-bit SuperH RISC, 32-bit multiplier)
  - PVcc = 3.0 to 3.6 V, Vcc = 1.1 to 1.3 V
- Operating frequency
  - CPU clock: 200 MHz
  - Bus clock: 66 MHz
- Internal memory
  - RAM: 32 KB
  - Cache memory: 16 KB
- DTCP-IP
- Host interface
  - 2 KB × 2 banks
  - HIF boot function
- Ethernet controller
  - EtherMAC (10/100 Mbps): 1
  - Transmit/receive FIFO: 512 Bytes each
  - TCP/IP checksum accelerator
- USB 2.0 High Speed
  - Host or Function: 1
- Memory interface
  - SRAM, SDRAM interface
  - External bus can be extended up to 32 bits.
- Encryption module
  - AES encryption/decryption
  - FIFO (independent transmit/receive)
  - Dedicated DMAC (AES FIFO ↔ SDRAM)
- MPEG-TS interface
  - PS
  - 2 channels included
- Peripheral functions
  - Serial communication interface with FIFO: 2
  - I^2C: 1 ch
  - SD host interface
  - 16-bit interval timer: 2
  - JTAG interface support, external interrupt pin, I/O port, etc.
- Package
  - BGA-240

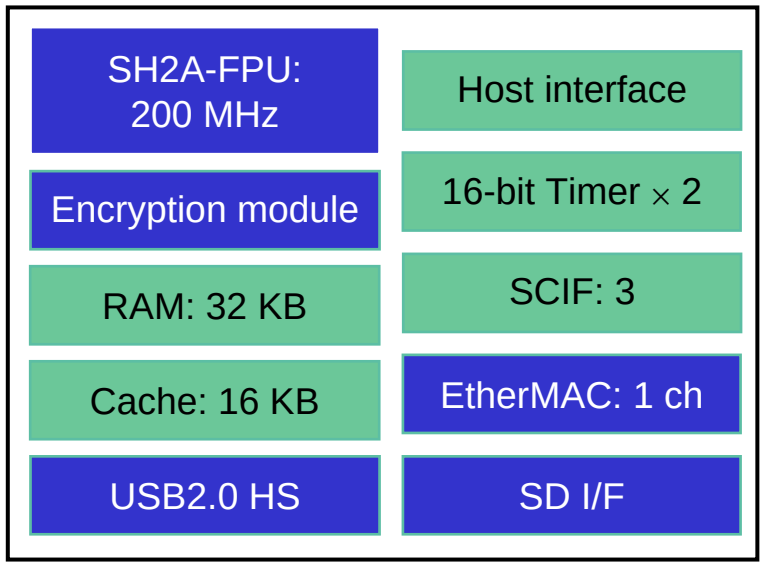
*The specification is subject to change.



Functional Overview of SH7670/SH7671/SH7672/SH7673

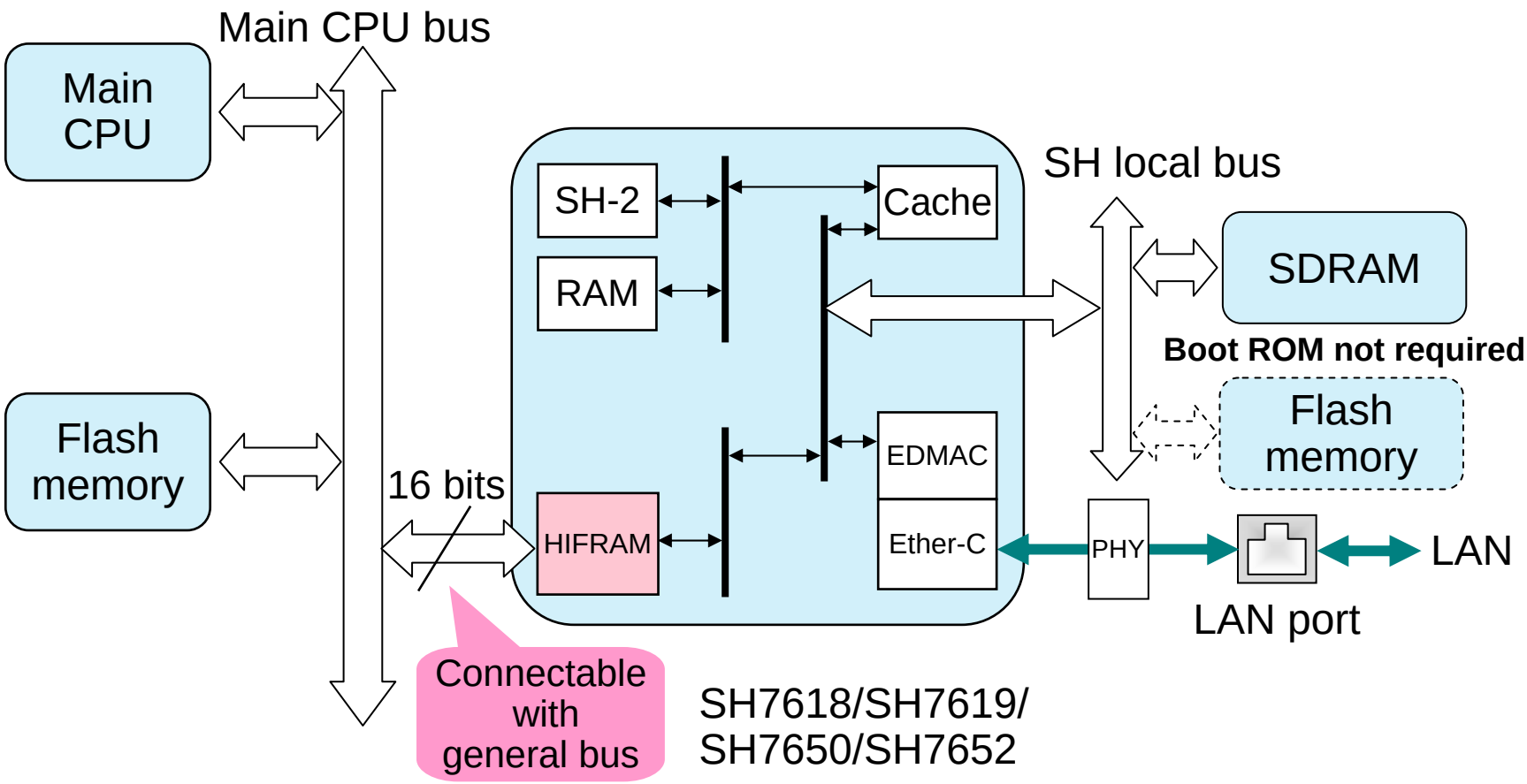
- CPU core
  - SH2A-FPU
    (32-bit SuperH RISC, 32-bit multiplier)
  - PVcc = 3.0 to 3.6 V, Vcc = 1.1 to 1.3 V
- Operating frequency
  - CPU clock: 200 MHz
  - Bus clock: 66 MHz
- Internal memory
  - RAM: 32 KB
  - Cache memory: 16 KB
- Host interface
  - 2 KB × 2 banks
  - HIF boot function
- Ethernet controller
  - EtherMAC (10/100 Mbps): 1
  - Transmit/receive FIFO: 512 Bytes each
  - TCP/IP checksum accelerator
- USB 2.0 High Speed
  - Host or Function: 1
- Memory interface
  - SRAM, SDRAM interface
  - External bus can be extended up to 32 bits.
- Encryption module (Only SH7672, 73)
  - AES encryption/decryption
  - FIFO (independent transmit/receive)
  - Dedicated DMAC (AES FIFO ↔ SDRAM)
- Peripheral functions
  - Serial communication interface with FIFO: 2
  - I^2C: 1
  - SD host interface (Only SH7671, 73)
  - 16-bit interval timer: 2
  - JTAG interface support, external interrupt pin, I/O port, etc.
- Package
  - BGA-256

*The specification is subject to change.



Host Interface (HIF)

Features:
1. Connectable to the main CPU with parallel bus
2. HIF boot function eliminates the need for boot ROM



SH7710/SH7712/SH7713 Overview

SH7712 is IPsec-less version of SH7710
SH7713 is IPsec-less, Ethernet (1) version of SH7710

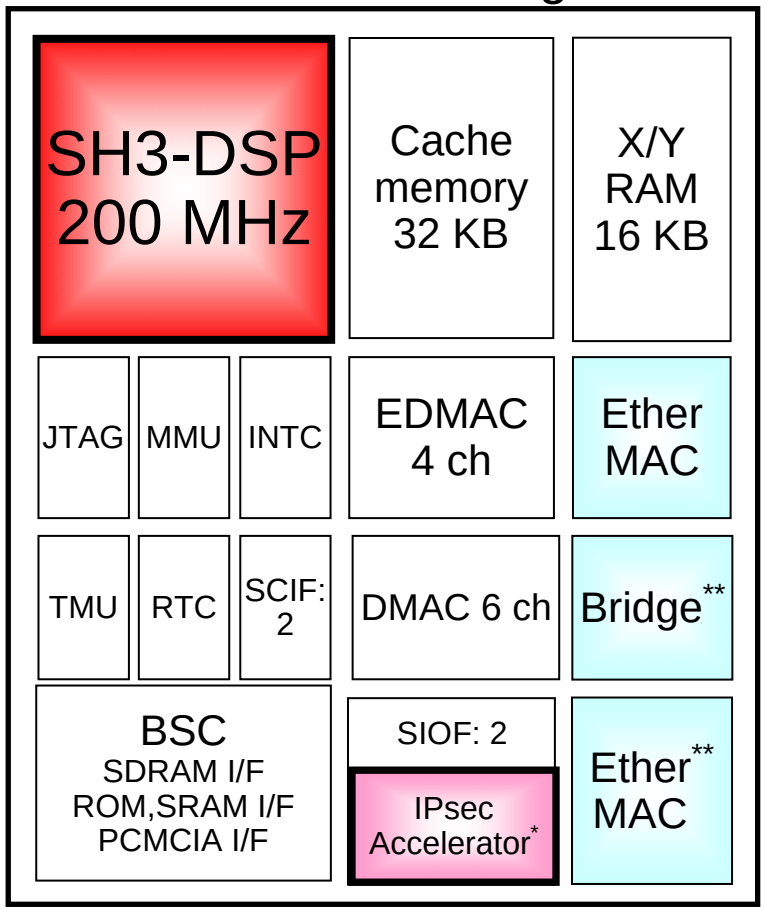
Features

- High performance RISC engine
  SH3-DSP core
  - 260 MIPS@200 MHz
- Ethernet Controller
  (MAC: IEEE802.3u compliant)
  - 10/100 Mbps, Full duplicate mode supported
  - Transfer/Receive FIFO: 2 KB each
  - Bridge: transfer FIFO: 3 KB each
- IPsec accelerator*
  - Authentication algorithm: SHA-1, MD5
  - Cryptography algorithm: DES, 3DES
  - Dedicated DMAC 4 ch
- Unified Cache: 32 KB
- Internal RAM: 16-KB X/Y-RAM
- SDRAM interface
- Power Supply Voltage: Core 1.5 V, I/O 3.3 V
- Package: QFP-256, CSP-256

Main applications

- Home gateway, VoIP-TA, IP phone,
  IP camera, Security equipment, etc

SH7710 Block Diagram



*: Only SH7710
**: Only SH7710 and SH7712

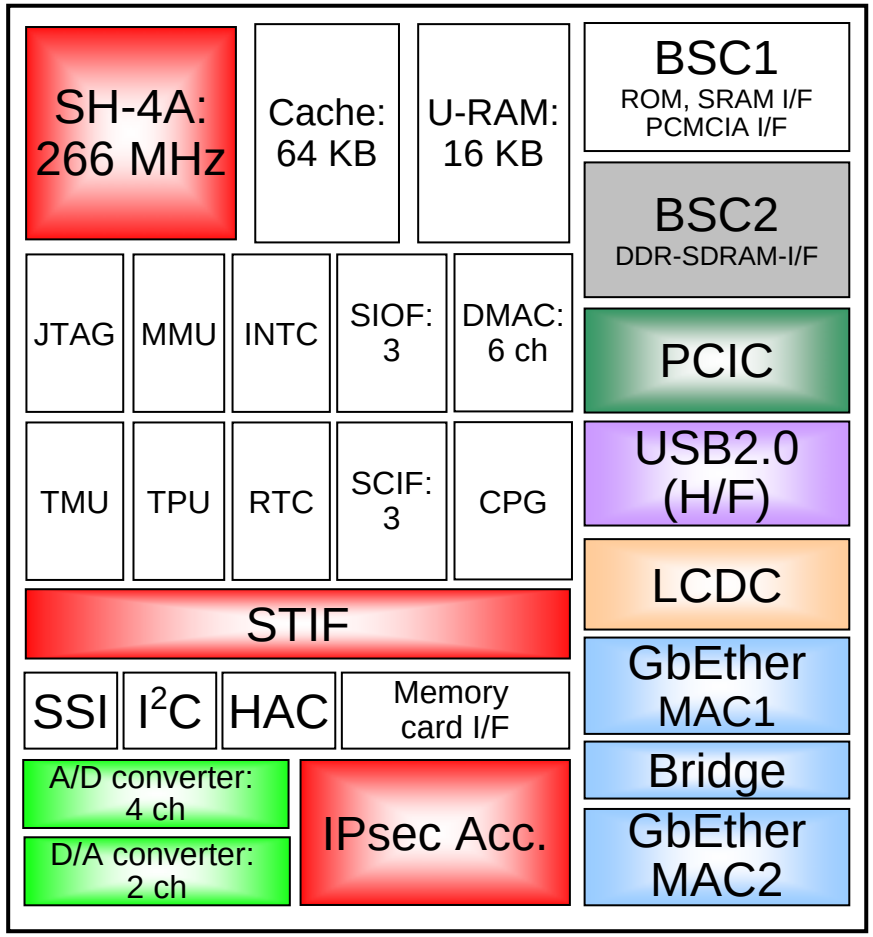
SH7763 Overview

Features

- SH4-A core (266 MHz)
- Cache (instruction: 32 KB, data: 32 KB)
- On-chip MMU
- 2-way super scalar 7-stage pipeline
- Internal RAM (16 KB)
- SDRAM interface
  Double data rate: 32-bit data bus,
  133 MHz (DDR266), Class 1
- On-chip STIF (stream interface)
- Ethernet controller (IEEE802.3): 2
  - 10/100/1000 Mbps full duplex transfer supported
  - Flow control (IEEE802.3x) supported
  - On-chip E-DMAC: 2 ch (Tx, Rx)
  - 2-KB send/8-KB receive FIFO
- IPsec accelerator
  - Authentification algorithm: SHA-1, MD5
  - Encryption algorithm: DES, 3DES, AES
  - On-chip IPsec DMAC: 2 ch
- PCI controller: PCI ver2.2
- LCD controller: VGA full color display is supported
- USB Host/Function: Ver. 2.0 Full Speed is supported
- Peripheral functions
  - SCIF (3), DMAC (6 ch), INTC, RTC, TMU, SIOF (3), SSI, I^2C, HAC, various memory card I/Fs, I/O ports, A/D converter, D/A converter, etc.
- Vcc
  - Core = 1.25 V, I/O = 3.3 V, DDR I/O = 2.5 V
- Package
  - PBGA2121-449, ball pitch: 0.8 mm

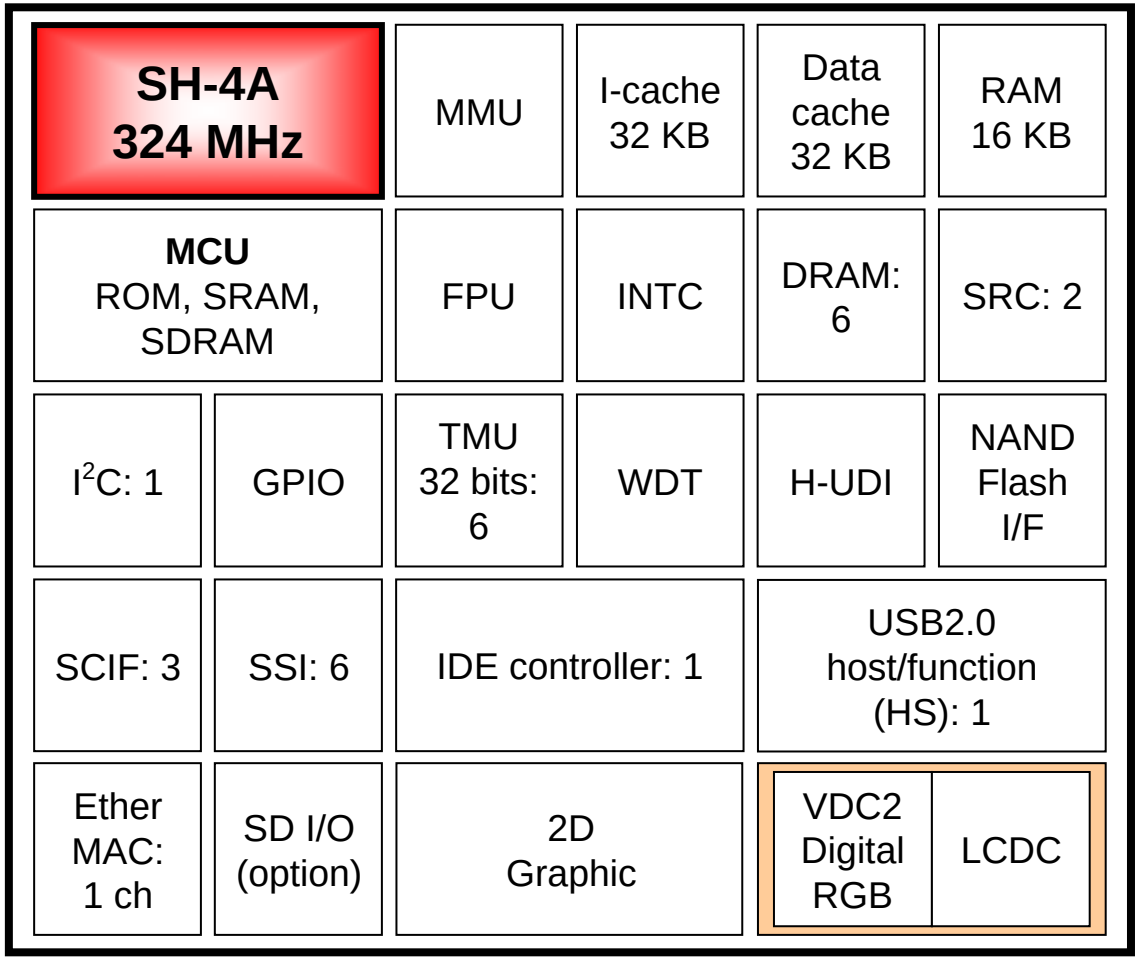
Block diagram of the SH7763

(Part No.: R5S77630Y-266BGV)



SH7764 Overview

- CPU core
  - SH-4A (SuperH RISC engine) FPU
- Operation frequency
  - CPU Clock: 324 MHz
  - Bus Clock: 108 MHz
- Operation Voltage (double voltage)
  - In 1.2 V/Ex 3.3 V
- Embedded memory
  - RAM: 16 Kbytes
  - Cache: I = 32 Kbytes
    D = 32 Kbytes
- Bus Interface
  - SRAM, Flash, SDRAM
  - External bus 8 bits, 16 bits, 32 bits (SDRAM: 32 bits/64 bits)
  - External bus space can be divided into 4 areas: Each 64 MB max. (Total 256 Mbytes)
- Peripheral
  - 32-bit Timer: 6
  - Watch dog Timer: 1
  - Ether MAC: 1 ch
  - I^2C bus interface: 1
  - DMA controller: 6 ch
  - SCIF (Asynchronous serial): 3
  - SSI (Codec I/F): 6
  - SCR (Sampling rate converter): 2
  - NAND Flash Interface
  - IDE controller (UltraDMA/66 Support): 1
  - SD I/O (option)
  - 2D Graphic
  - LCDC/Digital RGB (VDC2)
  - GPIO
  - INTC
  - H-UDI (User Debag Interface)
- Package
  - BGA404pin



List of Specifications for the SH-Ethernet Products (1)

Item	SH7615	SH7616	SH7618/18A	SH7619
	DSP function enhanced version	FIFO expanded version	EtherMAC	EtherMAC, PHY
CPU	SH2-DSP core		SH-2 core	
Operating frequency	62.5 MHz		100 MHz	125 MHz
Power supply voltage	3.3 V		1.5 V/3.3 V	1.8 V/3.3 V
Cache memory	4 KB		4 KB/16 KB	16 KB
Internal RAM	8 KB		4 KB	16 KB
General DMAC	2 ch		0	4 ch
Ethernet controller	1		1	1, PHY
Rx/Tx FIFO	512 B/512 B	2 KB/2 KB	SH7618: 256 B/256 B SH7618A: 512 B/512 B	512 B/512 B
Ethernet-specific DMAC	2 ch		2 ch	
User break controller	4		2	
Timer unit	3		2	
Free-run timer	1		0	
Serial communication I/F with FIFO	2		3	
Serial I/O	3		0	1
Package	208LQFP (SH7615ARF) 240CSP (SH7615ARBP)	208LQFP	176CSP	

List of Specifications for the SH-Ethernet Products (2)

Item	SH7710	SH7712	SH7713	SH7763	SH7764
	EtherMAC×2, IPsec	EtherMAC × 2	EtherMAC × 1	Gb EtherMAC × 2, PCI	EtherMAC × 1
CPU	SH3-DSP core			SH-4A core	SH-4A core
Operating frequency	200 MHz			266 MHz	324 MHz
Power supply voltage	1.5 V/3.3 V			1.25 V/3.3 V/2.5 V	1.25 V/3.3 V
Cache memory	32 KB			64 KB	64 KB
Internal RAM	16 KB			16 KB	16 KB
General DMAC	6 ch			6 ch	6 ch
Ethernet controller	2			2 (Gbit)	1
Rx/Tx FIFO	2 KB/2 KB × 2 pairs		2 KB/2 KB × 1 pair	8 KB/2 KB × 2 pairs	2 KB/2 KB × 1 pair
Ethernet-specific DMAC	4 ch		2 ch	4 ch	2 ch
User break controller	2			2	2
Timer unit	3			6	6
Free-run timer	-			-	-
Serial communication I/F with FIFO	2			3	3
Serial I/O	2 (incl.FIFO)			3 + USB (1)	6 + USB (1)
Package	HQFP2828-256 256CSP			PBGA2121-449	PBGA1919-404

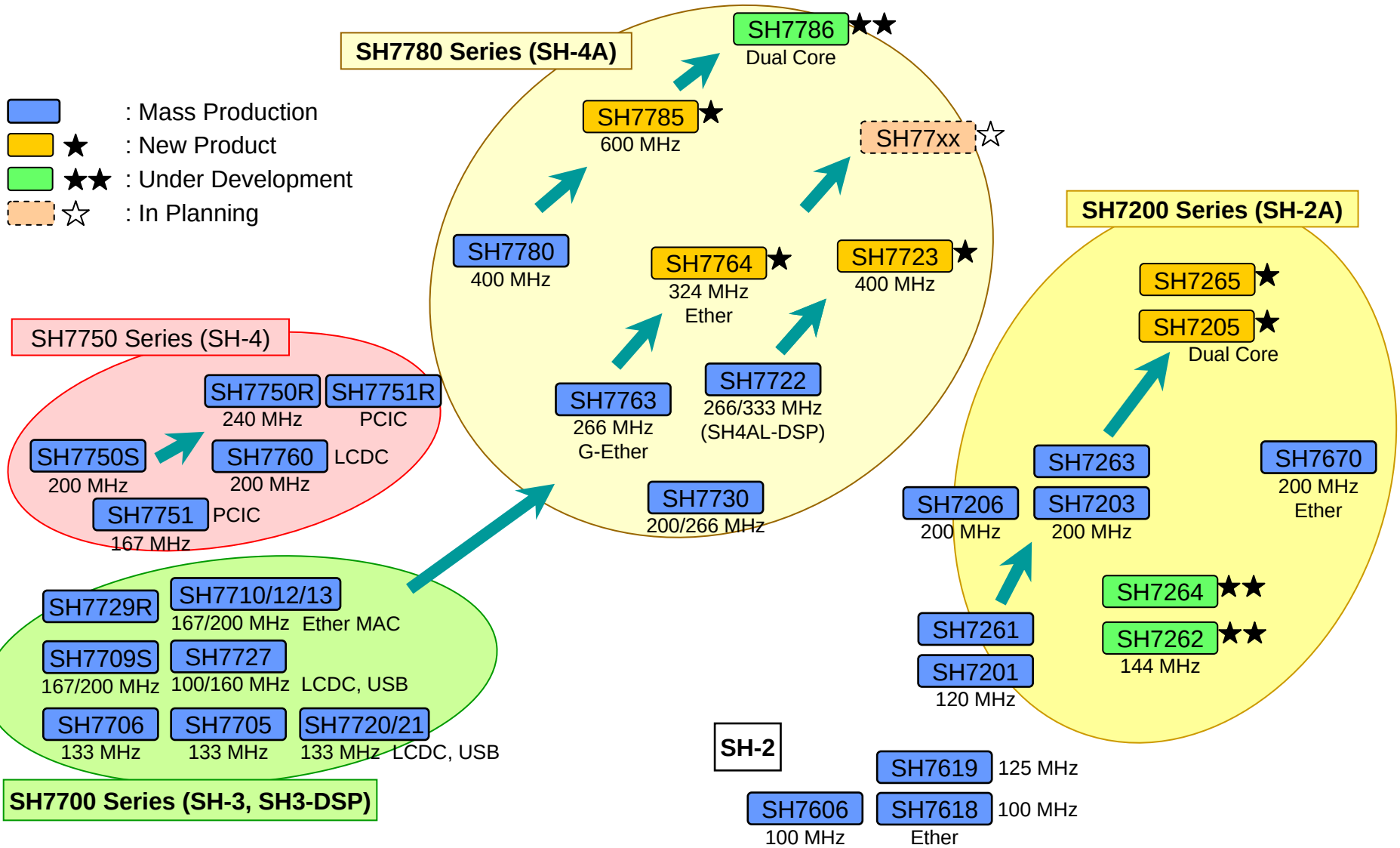
List of Specifications for the SH-Ethernet Products (3)

Item	SH7670	SH7671	SH7672	SH7673
	EtherMAC × 1	EtherMAC × 1, SDIO	EtherMAC × 1, Crypt	EtherMAC × 1, SDIO, Crypt
CPU	SH-2A core			
Operating frequency	200 MHz			
Power supply voltage	1.2 V/3.3 V			
Cache memory	16 KB			
Internal RAM	32 KB			
General DMAC	8 ch			
Ethernet controller	1			
Rx/Tx FIFO	512 B/512 B			
Ethernet-specific DMAC	2 ch			
User break controller	2			
Timer unit	2			
Free-run timer	-			
Serial communication I/F with FIFO	3			
Serial I/O	- (USB2.0 × 1)			
Package	256CSP			

Processor Type

SH7700 Series
SH7750 Series
SH7780 Series

Lineup of SuperH (Processor-Type) Microcontroller Products



High-Performance 32-Bit RISC Processor

Features

- Low power and high performance:

  133 mA@133 MHz (SH7705)
- MMU (Memory Management Unit), cache on chip
- Power management
  - Low-power mode
  - Frequency control
  - Module ON/OFF control
- Compatible with SH-1 and SH-2 instruction sets

SH7705 Overview

- SH-3 Low Power Version -

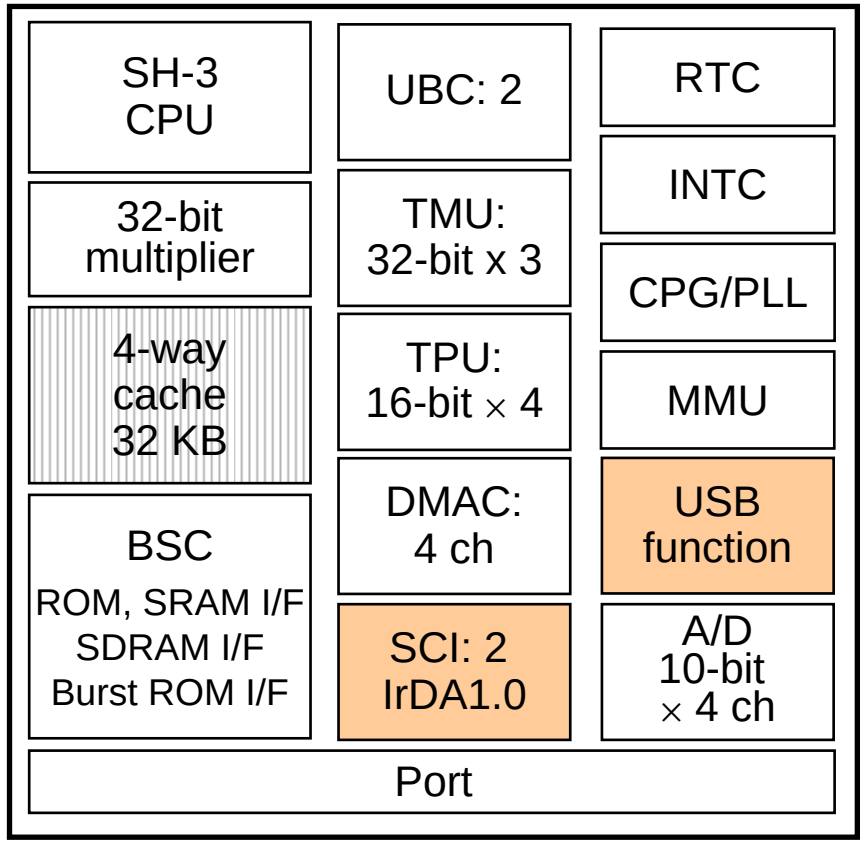
Features

- High-performance ultra-low power RISC CPU SH-3
  - Low power-consumption: 1 mA/MHz (typ.) @1.5 V (Internal)
  - CPU clock: 133 MHz/bus clock: 66 MHz
- Cache: Large Capacity 32 KB
- On-chip USB Function Ver.2.0 (Full Speed)
  - On-chip USB transceiver
  - Control/bulk/interrupt transfer support
- BSC (bus state controller)
  - Page mode FLASH, ROM, SRAM, SDRAM
- Enriched on-chip peripheral functions
  - DMAC, WDT, A/D Converter, CMT, RTC, etc.
- On-chip high-speed serial interface
  - UART/clock synchronous switchover type (on-chip 64-byte FIFO): 2 (IrDA1.0: 1)
- Powerful power management function
  - Sleep, standby, module standby, hardware standby
- Package: LQFP-208 (28 mm square), CSP-208 (12 mm square)

Main applications

- DSC, DVC, Video printer, Faxes, Ink-jet printer, Barcode Reader, PDA, and POS terminal

SH7705 Block Diagram



SH7706 Overview

- SH-3 Compact Version -

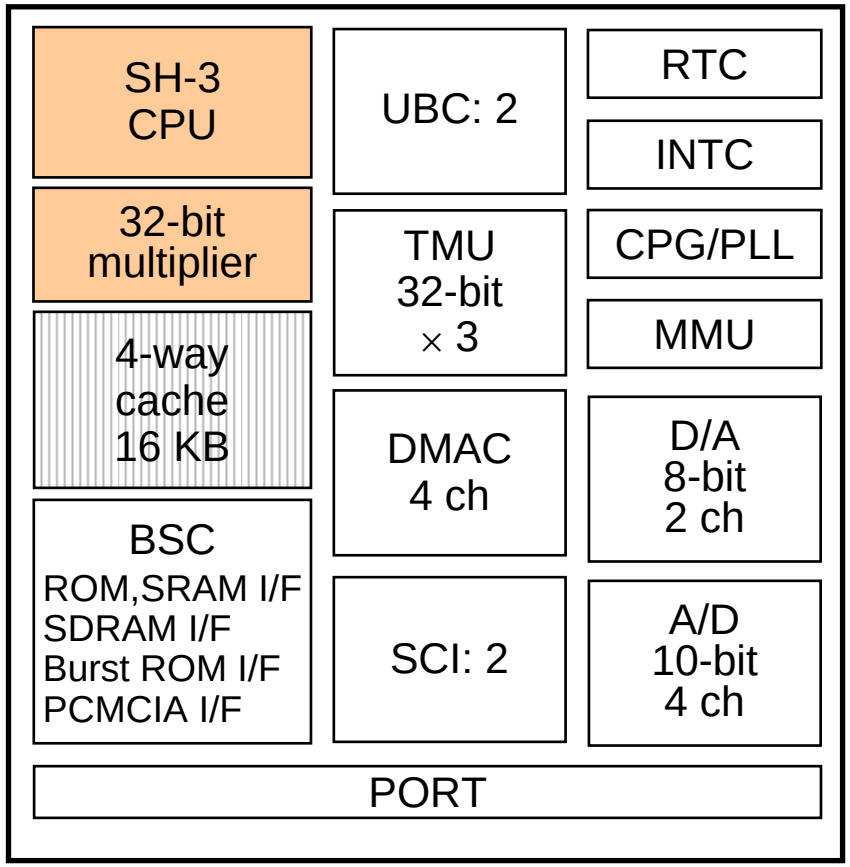
Features

- CPU SH-3: 133 MHz
- Cache: 16 KB
- Peripheral functions
  - 4-ch DMAC
  - 10-bit 4-ch A/D converter
  - 8-bit 2-ch D/A converter
  - SCI : 2 (with FIFO: 1)
  - 3-ch timer (32 bits)
  - RTC
- Power management function
- High-performance, low power consumption
- Package: 176-pin LQFP, 208-pin CSP

Main applications

- MFP/Ink-jet printers, Faxes, scanners, DVD recorders, and DVC

SH7706 Block Diagram



SH7709S Overview

- SH-3 High-speed Version -

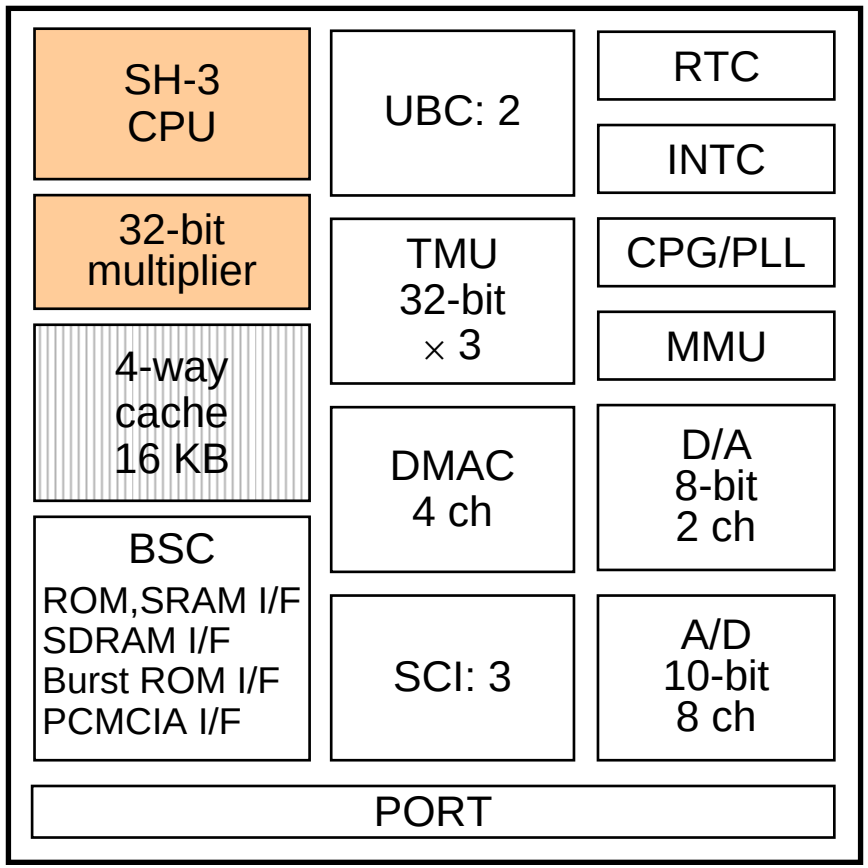
Features

- Improved CPU operation performance
  200 MHz (260 MIPS) MAX.
  Line-up is 100/133/167/200 MHz Version
- Cache: 16 KB
- Peripheral functions
  - 4-ch DMAC
  - 10-bit 8-ch A/D converter
  - 8-bit 2-ch D/A converter
  - SCI: 3 (with FIFO: 2)
    (IrDA 1.0: 1)
- Power management function
- High-performance and low power consumption
- Package
  - LQFP-208, CSP-240 (100/133/167 MHz)
  - HQFP-208 (200 MHz)

Main applications

- Portable information equipment, internet equipment, LBP, printer, scanner, and network equipment

SH7709S Block Diagram

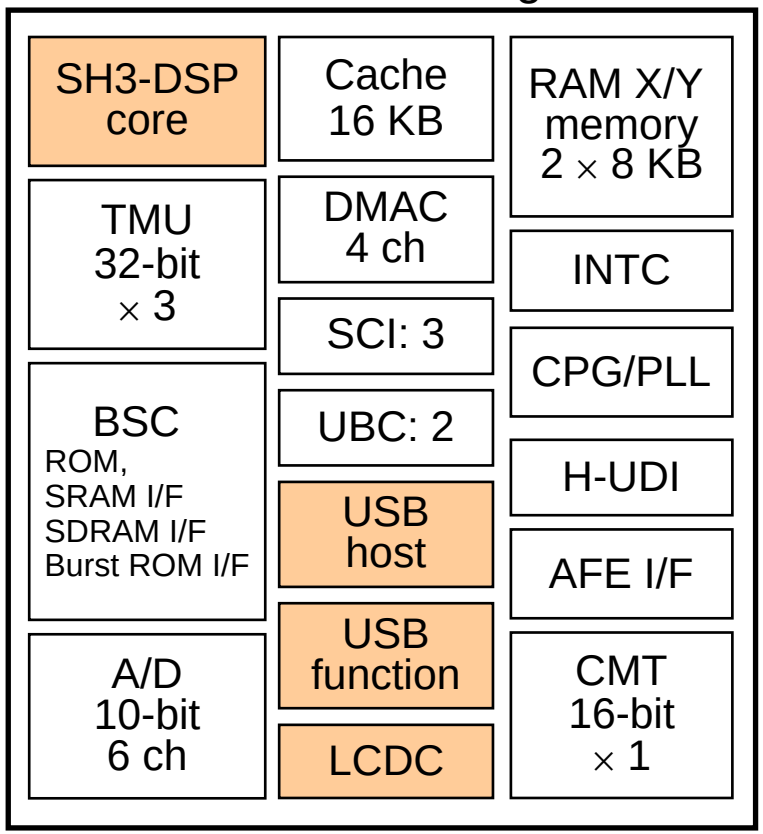


SH7727 Overview

Features

- Supports DSP instructions (16-bit fixed points)
  - to 100/160 MHz
  - to 200/320 MOPS
- MMU
- Cache: 16 KB
- X/Y memory (DSP core)
  RAM: 2 × 8 KB (total 16 KB)
- LCDC (color)
- USB function Ver.2.0 (Full Speed)
- USB host (Full/Low Speed),
  OHCI: Ver.1.0
- AFE interface
- Other functions: A/D converter and PCMCIA I/F etc
- On-chip debugger
  - JTAG interface H-UDI (subset)
  - User break controller (UBC)
- Package
  - HQFP-240
  - CSP-240

SH7727 Block Diagram



Main applications

- Faxes, printer, AV equipment terminal, webphone, POS terminal, internet terminal, and DSC printer.

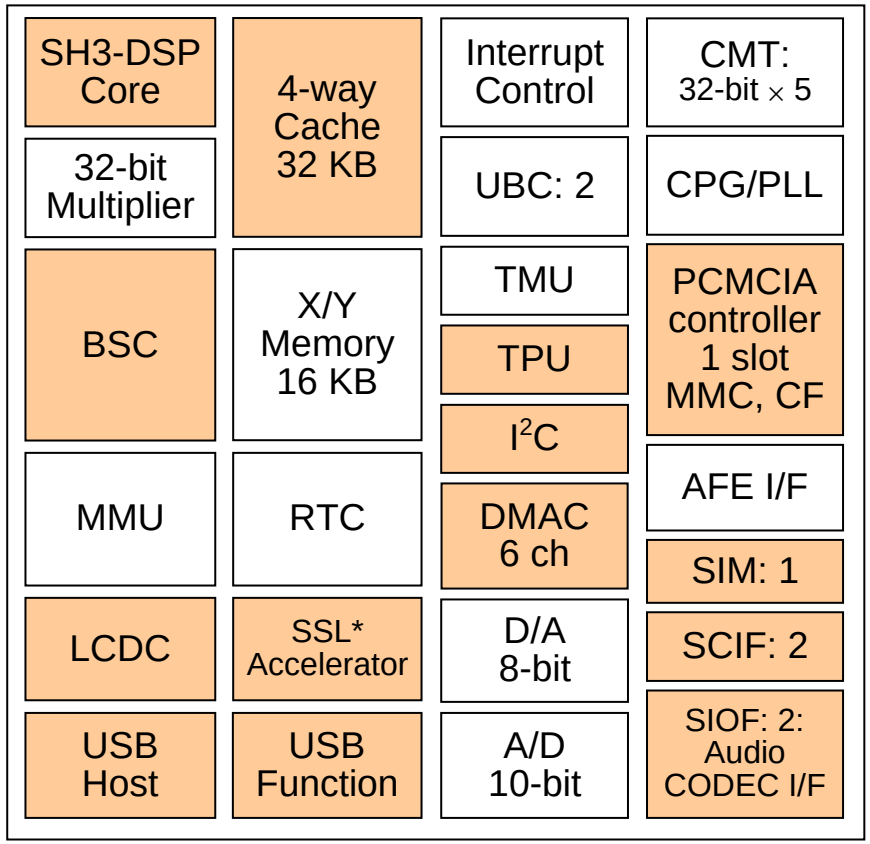
SH7720/SH7721 Overview

SH7721 is SSL-less version of SH7720

Features

- Supports DSP instructions (16-bit fixed points)
  - to 133 MHz
  - to 266 MOPS
- MMU
- Cache 32 KB
- SSL accelerator
- X/Y memory (DSP core)
  RAM: 2 × 8 KB (total 16 KB)
- LCDC (color)
- USB function (Ver. 2.0 Full Speed)
- USB Host (Full/Low Speed)
  OHCI: Ver.1.0
- I^2C bus interface:
- DMAC × 6 channels
- TMU: 32-bit timer × 3
- TPU: 16-bit timer × 4
- SCIF: Serial interface with FIFO × 2
- IrDA interface (Ver. 1.0)
- SIOF: Audio serial interface with FIFO × 2
- Smart Card Interface
- AFE I/F
- A/D converter 10-bit × 4 ch,
  D/A converter 8-bit × 2 ch
- PCMCIA I/F, MMC I/F
- Package: FBGA-256
  (17 mm × 17 mm, ball pitch: 0.8 mm)
  (11 mm × 11 mm, ball pitch: 0.5 mm)

SH7720 Block Diagram



*: only SH7720

Main applications

- IP Phone, Faxes, Printer, AV equipment terminal, Webphone
  POS terminal, Internet terminal, and DSC printer

SH7729R Overview

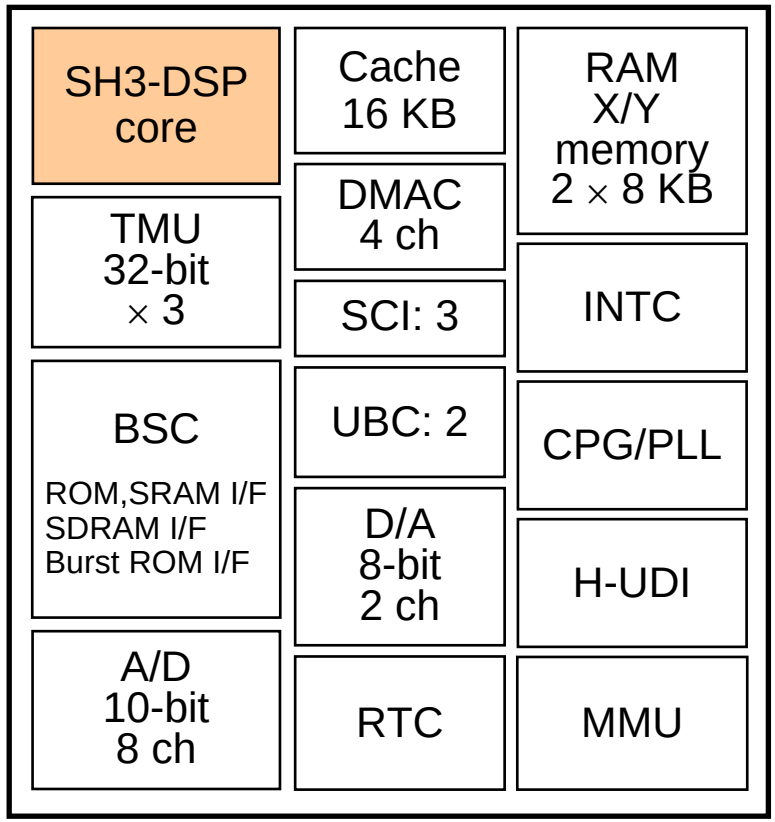
Features

- DSP instruction (SH3-DSP)
  - 100 MHz/133 MHz/167 MHz/200 MHz
  - 200 MOPS/266 MOPS/334 MOPS/400 MOPS
- MMU
  - MMU fully compatible with the SH-3 (TLB)
- Cache
  - Cache fully compatible with the SH-3 (16 KB)
- Built-in memory for DSP processing (X/Y memory)
  - RAM: 2 × 8 KB (total 16 KB)
- Built-in debugging function
  - Emulation interface that conforms to JTAG (H-UDI)
  - User break controller (UBC)
- Package
  - LQFP-208, CSP-240 (100/133/167 MHz)
  - HQFP-208 (200 MHz)

Main applications

- Network application (VoIP), internet FAX, webphone, DSC, and TV conference system

SH7729R Block Diagram



Multimedia SH-4/SH4-A RISC Processor

Features

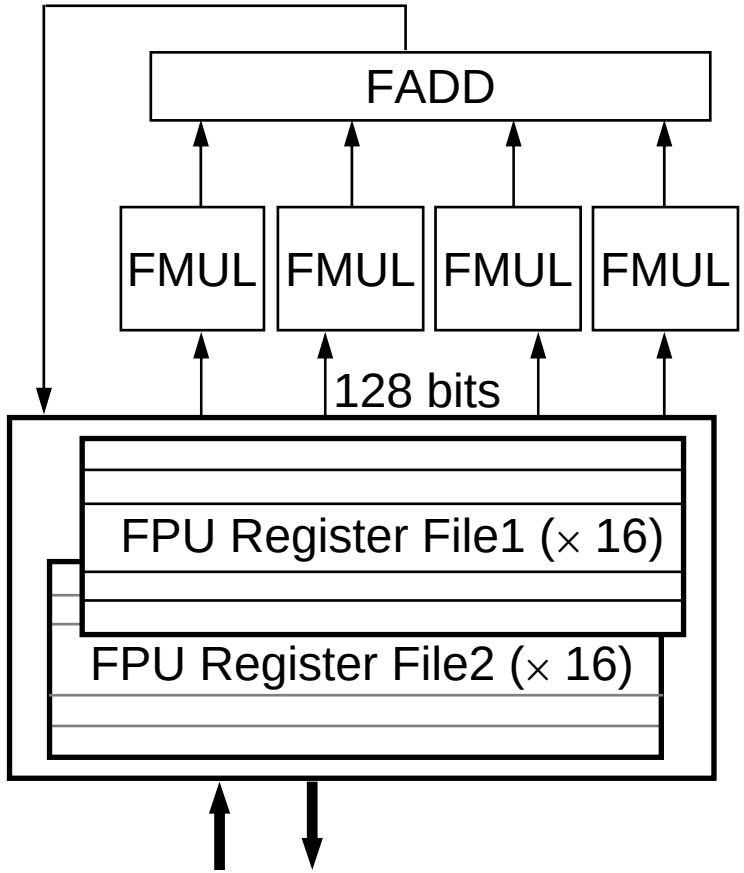
- High performance CPU that enables parallel execution of two instructions
- Ultra-high-speed 3D vector multiplier
- Upwardly compatible with SH-1/SH-2/SH-3 instruction sets
  - 16-bit fixed-length instructions
  - IEEE754 floating-point instructions are supported (high-speed single precision and double precision)

Ultra-High-Speed Floating-Point Operation

FTRV instruction XMTRX, FVn

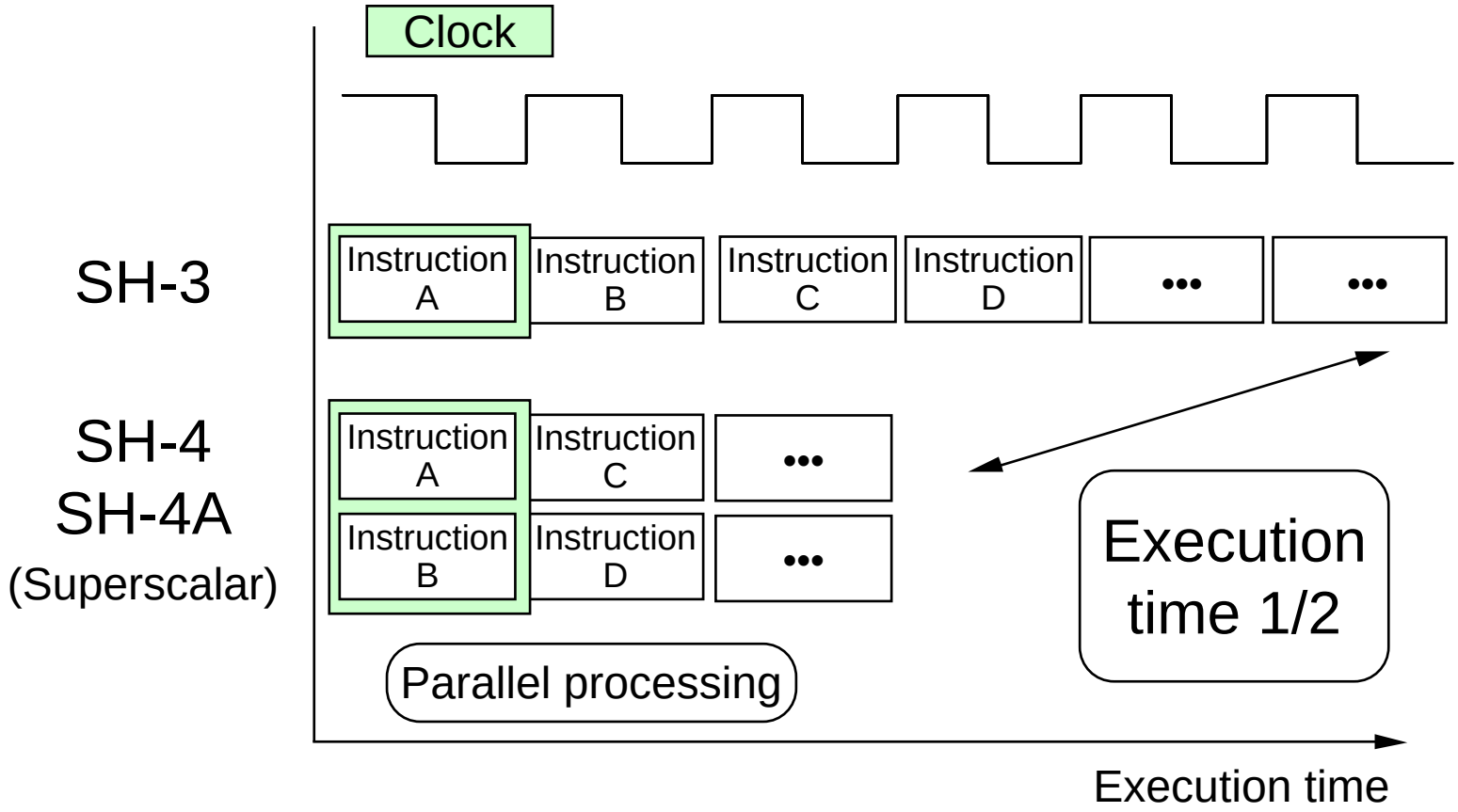
$$\begin{pmatrix} a11 & a12 & a13 & a14 \\ a21 & a22 & a23 & a24 \\ a31 & a32 & a33 & a34 \\ a41 & a42 & a43 & a44 \end{pmatrix} \times \begin{pmatrix} x \\ y \\ z \\ i \end{pmatrix} = \begin{pmatrix} x' \\ y' \\ z' \\ i' \end{pmatrix}$$

- 16 multiplications and 12 additions are executed in four clock cycles
- Loading/storing to other registers during an operation is possible



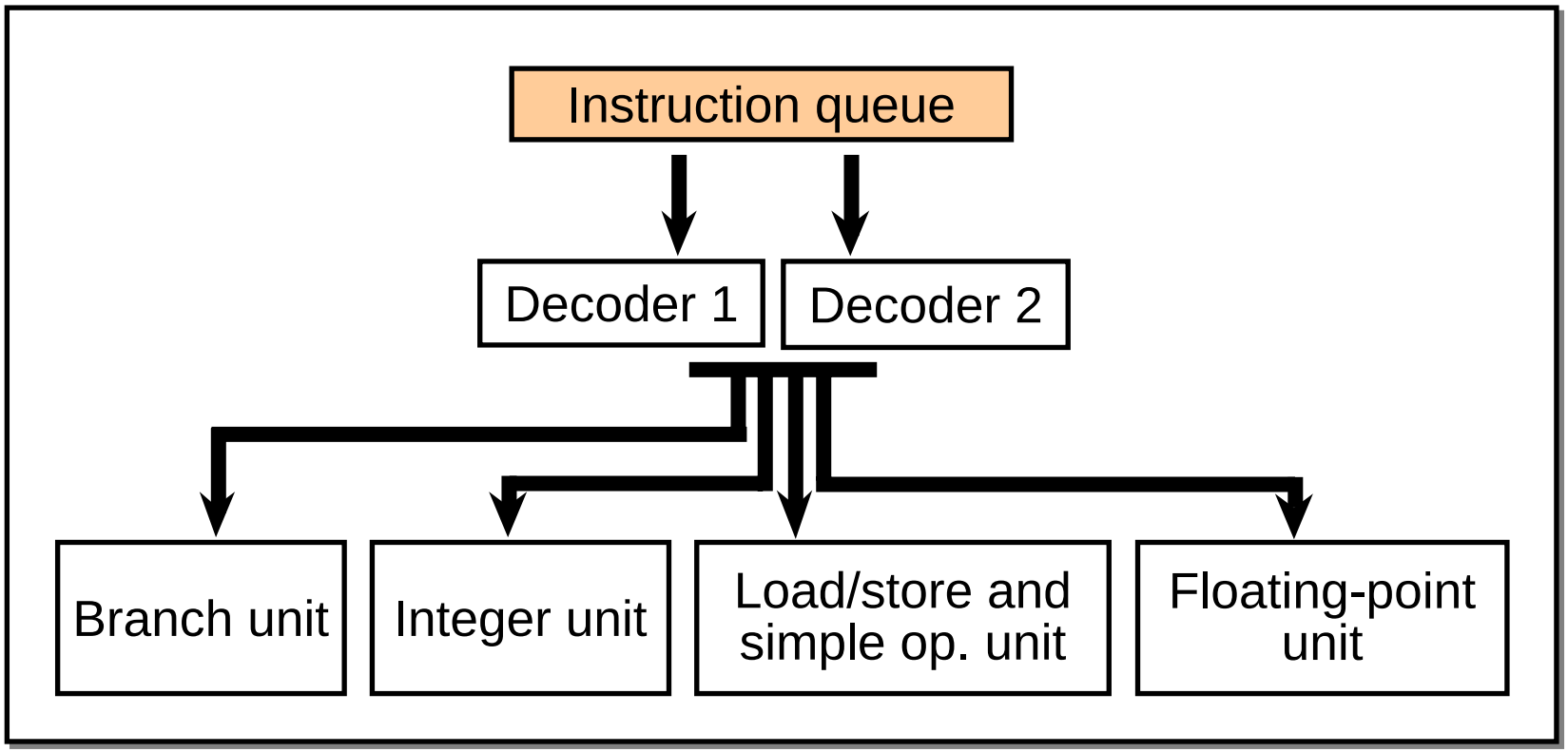
Features of SH-4

- Superscalar -



2-Way Superscalar Method

- 2-instruction parallel execution
- Improved execution efficiency with simple hardware



SH7750R Overview

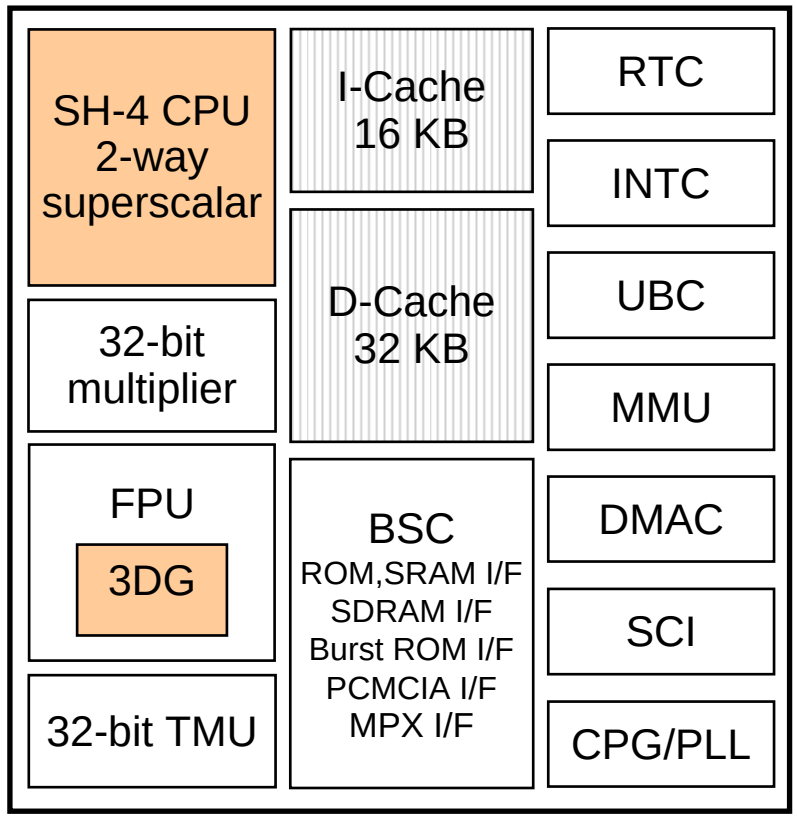
- 2-way superscalar architecture -

Features

- High-performance 2-way superscalar
- Operating frequency: 200/240 MHz
  - Internal power supply voltage: 1.5 V (typ.)
- Built-in MMU
- Cache: (Harvard architecture)
  - large-capacity cache:
    16-KB instruction + 32-KB data
    (2-way set associative)
- DMAC: 8 channels
- When bus width is 64 bits, 256-Mbit SDRAM ($\times$ 16) is supported
- Package:
  BGA-256, QFP-208
  BGA-292 (17 mm $\times$ 17 mm, 0.8-mm pitch)

Main applications

- Car navigation, image processing, STB, digital TV, and printer



SH7751R Overview

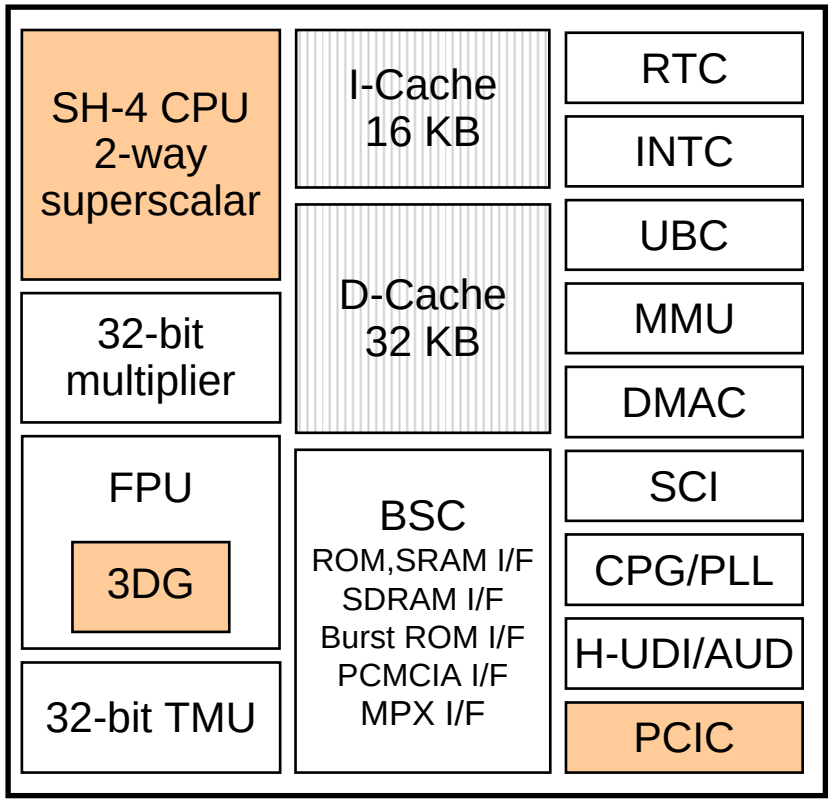
- SH-4 on-chip PCI version -

Features

- High-performance 2-way superscalar
- Operating frequency: 200/240 MHz
  - Internal power supply voltage: 1.5 V (typ.)
- Built-in MMU
- Cache: (Harvard architecture)
  - large-capacity Cache:
    16-KB instruction + 32-KB data
    (2-way set associative)
- DMAC: 8 channels
- Package:
  BGA-256, QFP-256
  BGA-292 (17 mm × 17 mm, 0.8-mm pitch)

Main applications

- Communications
  - Routers, PBX, LAN/WAN, and NAS
- OA/PC peripherals
  - Printer, scanner, and PPC

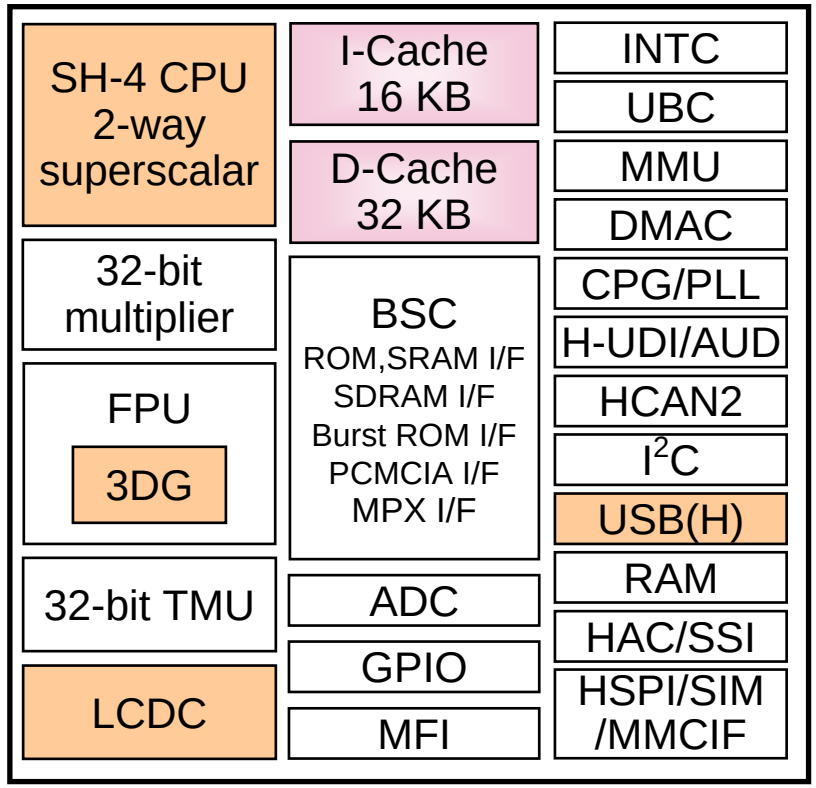


SH7760 Overview

- High-performance processor with on-chip LCD controller and USB host -

Features

- High-performance 2-way superscalar
- Operating frequency:
  200 MHz (Internal)/66 MHz (Bus)
  - Internal power supply voltage: 1.5 V (typ.)
- Large-capacity Cache:
  16-KB instruction + 32-KB data
  (2-way set associative)
- Peripheral modules
  - LCDC: LCD controller (640 × 480: 256 colors, etc.)
  - USB: USB host (Full/Low Speed)
  - OHCI: Ver.1.0
  - SCIF, HAC, SSI, I^2C, HSPI, SIM, MMCIF, CMT, A/D Converter, MFI, and GPIO
- Package:
  BGA-256 (17 mm × 17 mm, 0.8-mm pitch)



Main applications

- Car navigation, Telematics

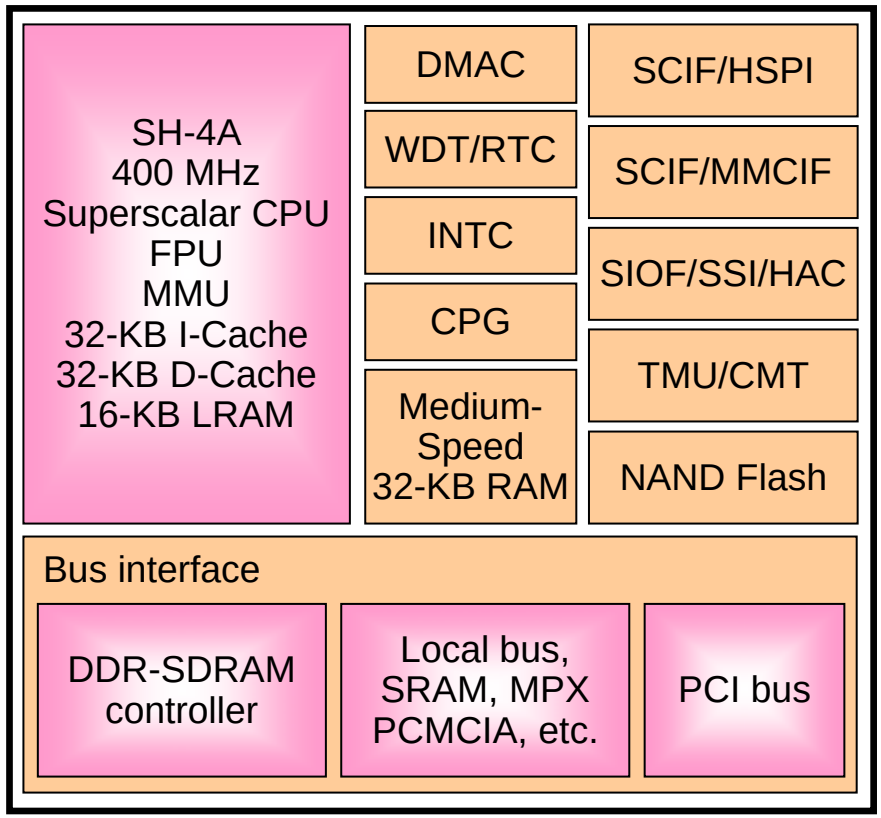
SH7780 Overview

Features

- CPU core
  - CPU core: SH-4A
  - Operating frequency: 400 MHz@1.25 V
- External bus interface (3-bus configuration)

	Voltage	Bus width	Clock frequency
- DDR I/F	2.5 V	32 bits	160 MHz
- Local bus	3.3 V	32 bits	100 MHz
- PCI	3.3 V	32 bits	33/66 MHz

- Cache memory/Internal memory
  - Instruction cache: 32 KB (4-way set associative)
  - Data cache: 32 KB (4-way set associative)
  - LRAM(high-speed): 16 KB
  - Medium-speed RAM: 32 KB
- Peripheral modules
  - DMAC: 12 ch
  - SCIF: 2
  - SIOF/SSI/HAC
  - NAND flash controller
  - MMCIF
- Package:
  BGA-449 (21 mm × 21 mm, 0.8-mm pitch)



Main applications

- Car navigation, amusement equipment, network terminals, laser-beam printers

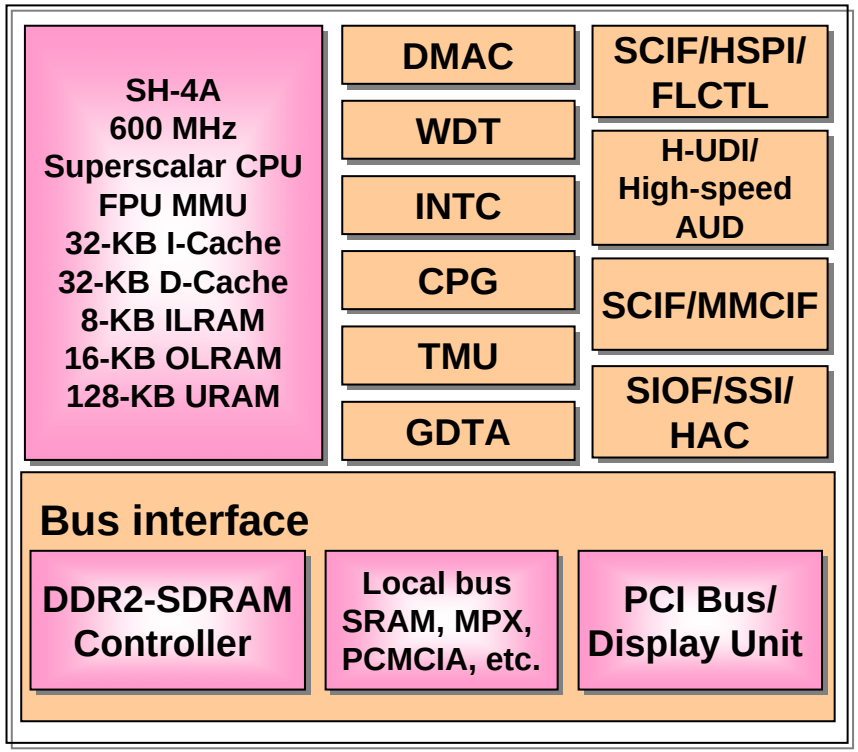
SH7785 Overview

Features

- CPU core
  - CPU core: SH-4A
  - Operating frequency: 600 MHz@1.1 V
- External bus Interface (3-bus configuration)

	Voltage	Bus width	Clock frequency
- DDR I/F	1.8 V	32 bits	300 MHz
- Local bus	3.3 V	32/64 bits	100 MHz
(64-bit width when PCI bus/display unit are not in use)			
- PCI	3.3 V	32 bits	33/66 MHz

- Cache memory/Internal memory
  - Instruction cache: 32 KB (4-way set associative)
  - Data cache: 32 KB (4-way set associative)
  - LRAM (high speed): 8 KB + 16 KB
  - URAM (middle speed): 128 KB
- Peripheral modules
  - Display unit (DU)
  - Data translation accelerator (GDTA)
  - DMAC: 12 channels
  - SCIF, HSPI, and NAND Flash memory controller
  - SIOF, SSI, and HAC
  - MMCIF
  - H-UDI, high-speed AUD
- Package: BGA-436 (19 mm × 19 mm, 0.8-mm pitch)



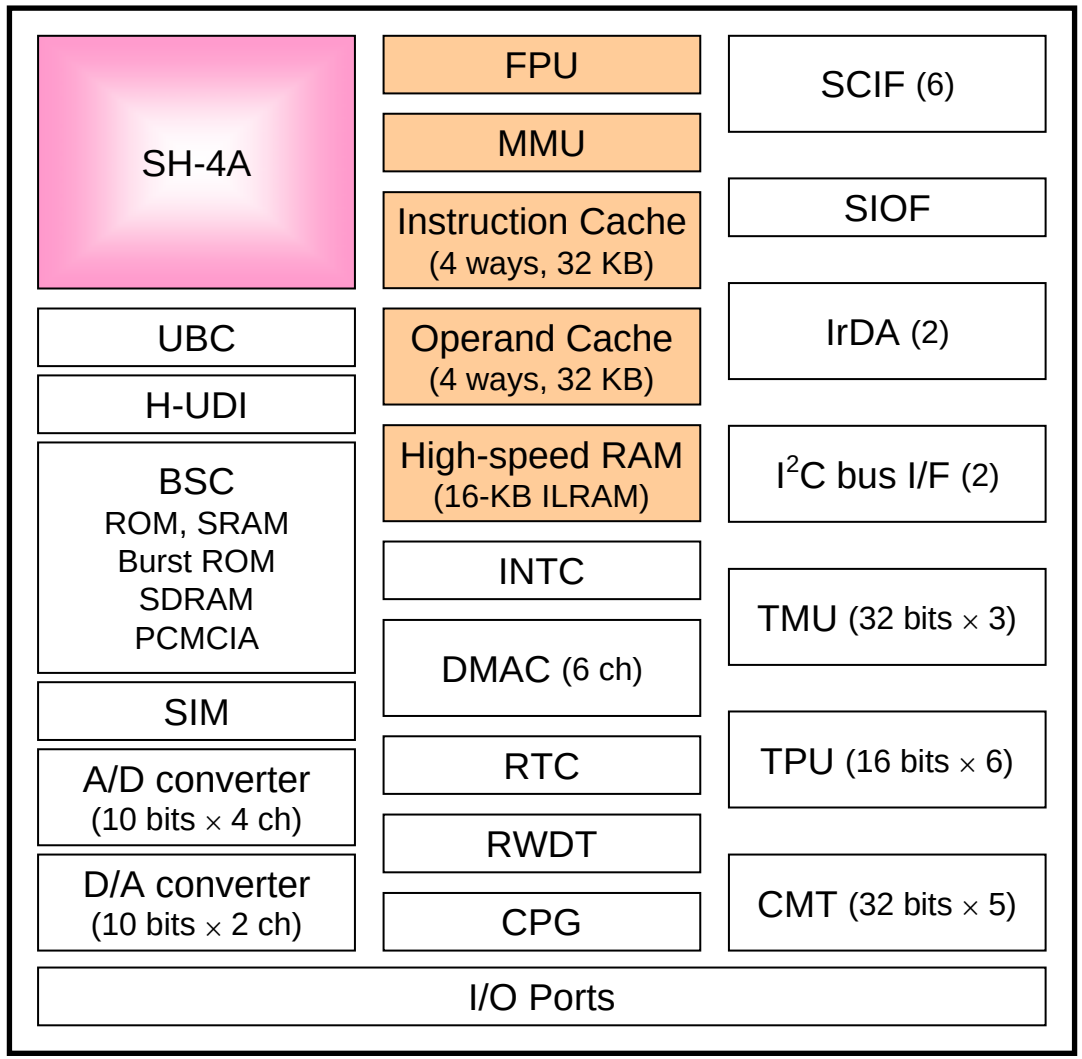
Main applications

- Car navigation systems, amusement devices, network terminals, LBPs (laser beam printers), etc.

Overview of the SH7730

Features

- High-performance CPU: SH-4A
  - Operating @ 266/200 MHz (480/360 MIPS)
  - On-chip FPU, Support for MMU
- On-chip cache memory
  - Instruction cache: 32 KB
  - Operand cache: 32 KB
- Internal memory: 16 KB (ILRAM)
- External bus: 32 bits, 66 MHz
  - ROM/SRAM
  - SDRAM
- Peripheral modules
  - DMAC: 6 ch
  - Various timers (TMU, TPU, and CMT)
  - SCIF: 6 (IrDA: 2, SIOF: 1)
  - I^2C: 2
  - A/D converter: 10 bits, 4 ch
  - D/A converter: 10 bits, 2 ch
- Power management function
  - Sleep module standby
  - software standby
- On-chip debugging
- Package:
  208-pin QFP (28 mm × 28 mm)

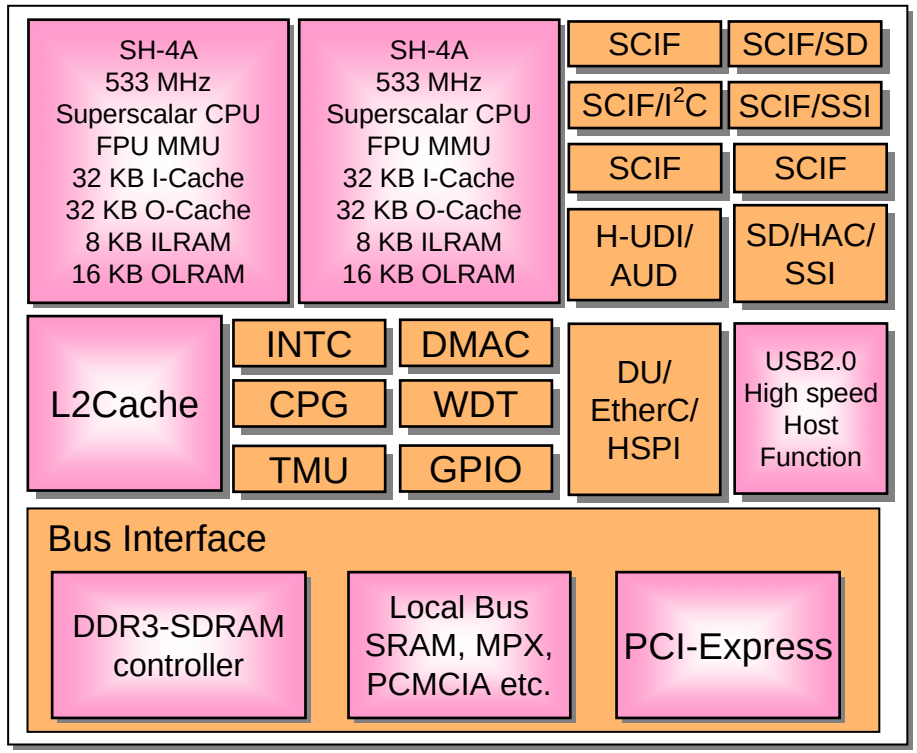


SH7786 Overview

Under Development

Features

- CPU Core
  - CPU Core: SH-4A × 2
  - Frequency: 533 MHz@1.25 V
- External bus Interface
  - DDR3 I/F: 32 bits width (max.)
    : 533 MHz (max.)
  - Local Bus: 8/16/32 bits width
    : 88.9 MHz (max.)
  - PCI-Express: (4 lane + 1 lane) or
    (2 lane + 1 lane + 1 lane)
- Cache memory/Internal RAM
  - I-Cache: 32 KB × 2
  - O-Cache: 32 KB × 2
    : Cache snoop function
  - LRAM (High speed): (8 KB + 16 KB) × 2
  - L2Cache: 256 KB
- Peripheral module
  - Display Unit (DU): 1 ch (max.)
  - USB2.0 High speed: 2 ch (max.) (Host/Function)
  - Ethernet Controller: 1 ch (max.) (MII Interface)
  - DMAC: 24 ch (max.)
  - SDIF: 2 ch (max.)
  - SCIF: 6 ch (max.)
  - I^2C: 2 ch (max.)
  - HSPI, SSI, HAC, NAND controller, H-UDI, AUD
- Package: BGA-593 (25 mm × 25 mm: 0.8 mm pitch)

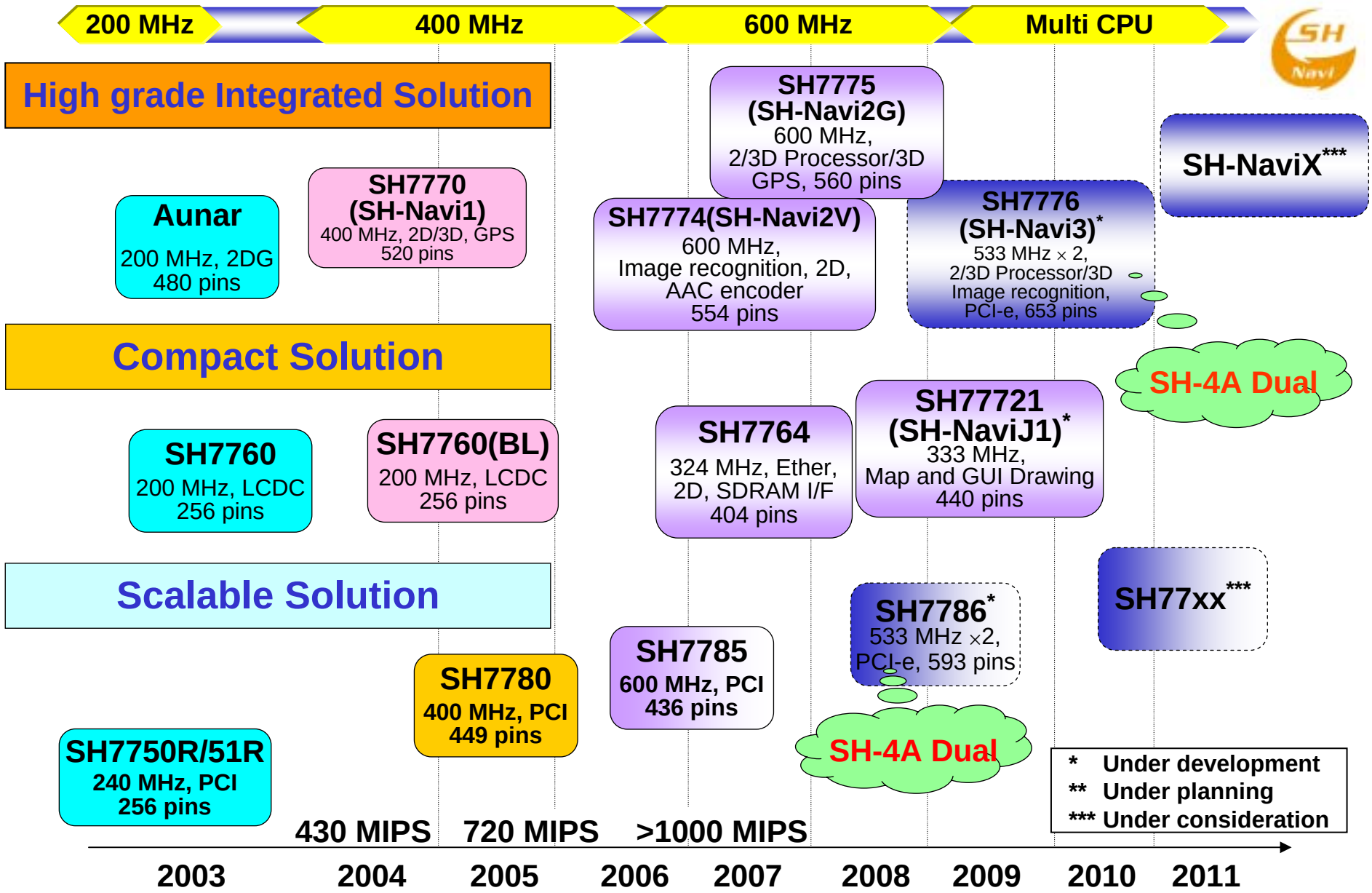


Main Application

- Car navigation, amusement device, Network terminals

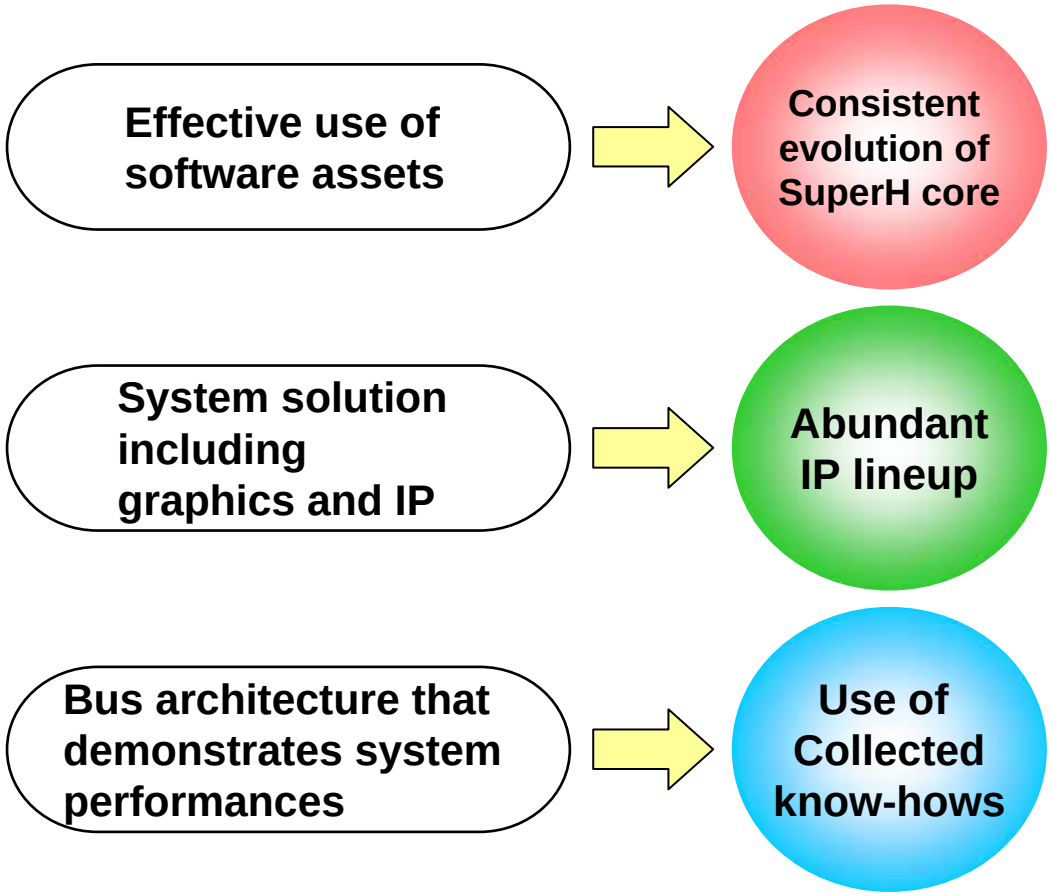
SuperH for Car Infotainment System

Roadmap of SH-4/SH-4A Product for CIS



SH7770 for Full Graphics Display Type In-Vehicle Terminal

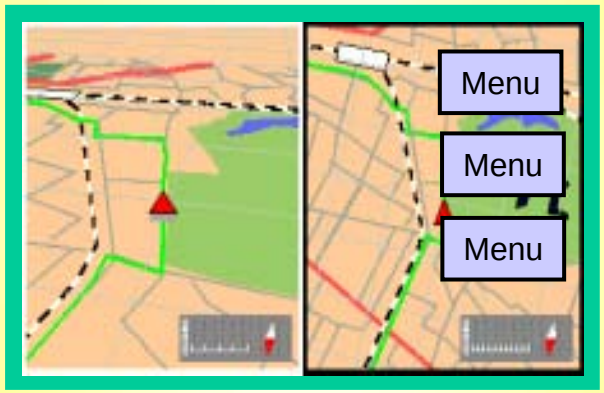
- All-in-one chip with graphics accelerator
- Introduction of 400-MHz SH-4A core realizes the high performance of processing



Display Example of SH7770 2D/3D Graphics

- **SH7770 have an exclusive accelerator of 2D/3D individually.**

2D Graphic



e.g.) Map-Drawing

3D Graphic

Translucency and reflections

Bumpmap

True-color blending

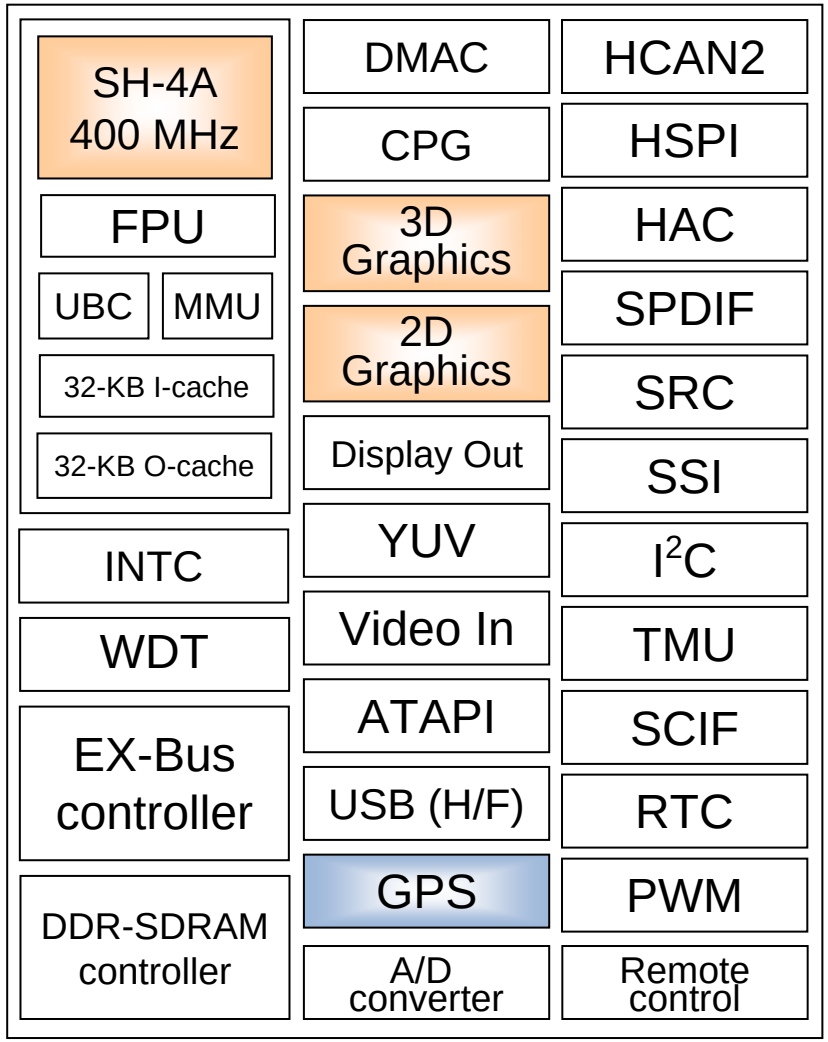
* 3D graphics IP from Imagination Technologies, Ltd. of the United Kingdom is used as the on-chip 3D graphics engine

SH7770 Overview

SH7770

Features

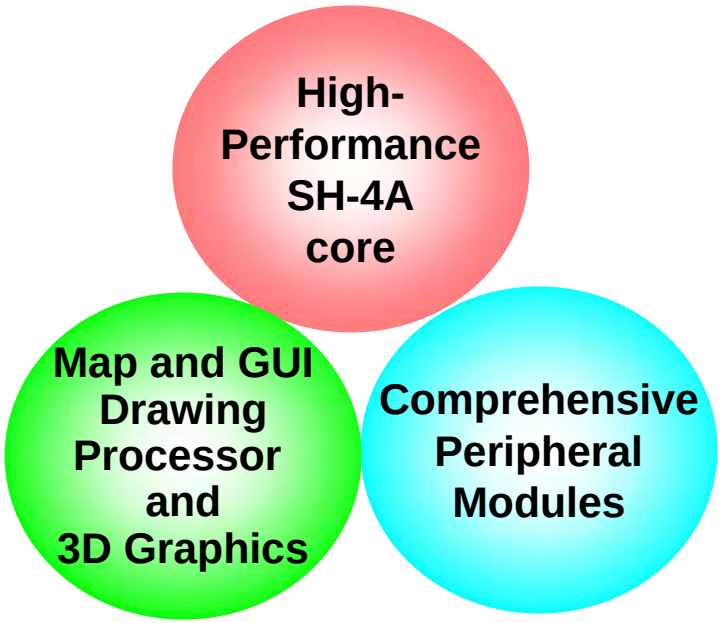
- Max. internal operating frequency of SH-4A core:
  400 MHz
- Power supply voltage:
  3.3 V (I/O), 2.5 V (DDR), 1.25 V (core)
- Performance:
  720 MIPS (Dhrystone) @400 MHz
- 2-way superscalar, 7-stage pipeline
- Cache:
  32-KB 4-way set associative (I-, O-cache)
- Memory: DDR SDRAM I/F
- 2D Graphics Engine
- 3D Graphics Engine
- Display:
  WVGA 854 dots × 480 dots (16-bit pixel)
- Peripheral functions:
  Please refer to the diagram at right.
- Package: BGA-520 pins
  (33 mm × 33 mm, 1.0-mm pitch)

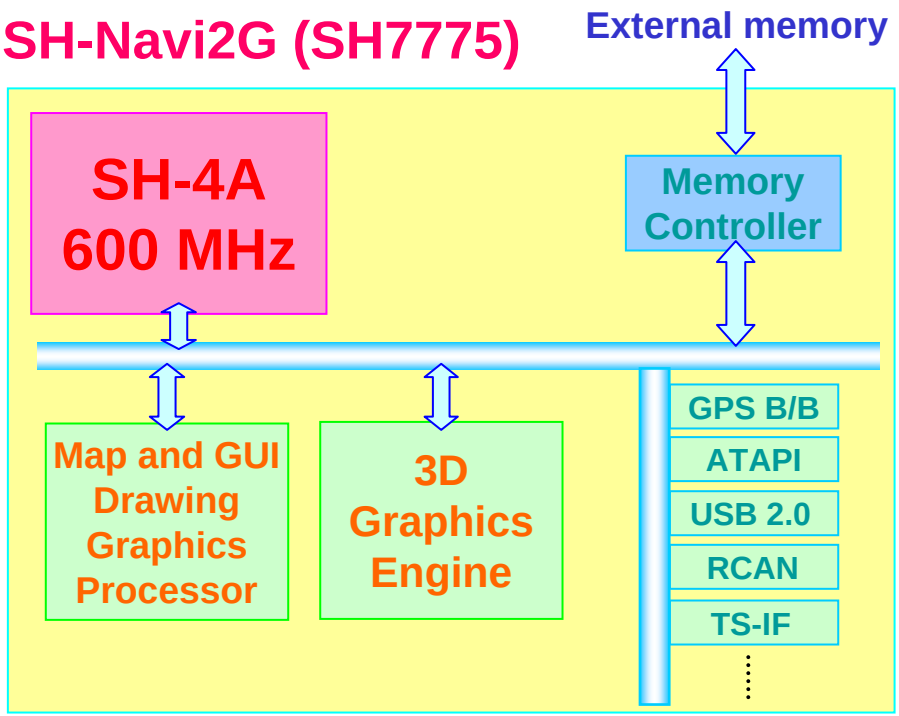


SoC SH-Navi2G “SH7775” for Car Navigation System

- **High performance SoC equipped with Map and GUI Graphics Processor, 3D Graphics Engine, and various function for car navigation system.**

Product concept





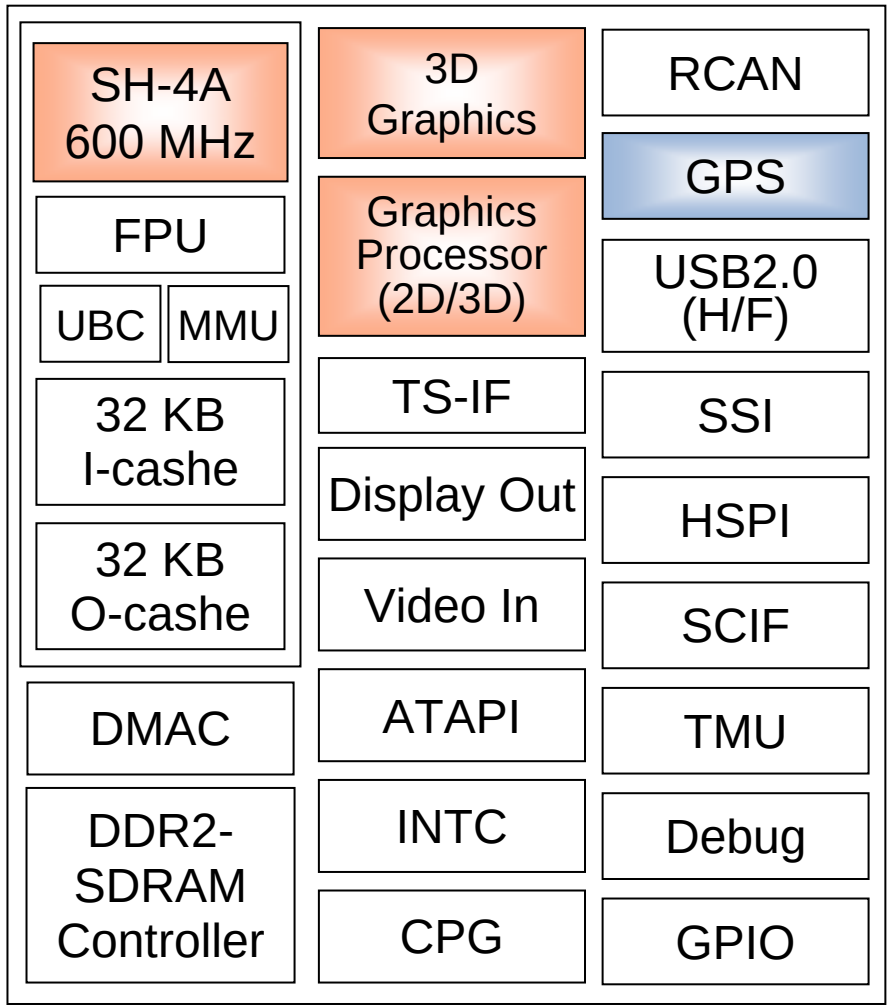
1. SH-4A CPU core operating at 600 MHz with 50% increase of current Renesas SoC products
2. Newly developed on-chip Graphics Processor optimized for Map and GUI Drawing and 3-D Graphics Engine.
3. Comprehensive range of peripheral functions for car information systems

SH7775 Overview

SH7775

Features

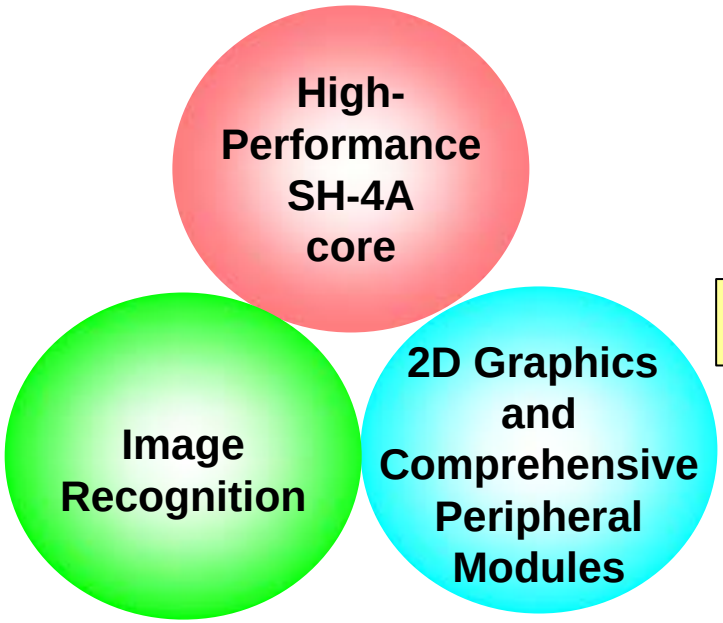
- Max. internal operating frequency of
  SH-4A core: 600 MHz
- Power supply voltage:
  3.3 V (I/O), 1.8 V (DDR), 1.1 V (Core)
- Performance:
  1080 MIPS@600 MHz
- Cache:
  32-KB 4-way set associative (I-, O-cache)
- Memory: DDR2 SDRAM I/F
- Renesas Graphics Processor (2D, 3D)
- 3D Graphics Engine
- Display:
  WVGA 832 dots × 496 dots (16-bit pixel)
- Peripheral functions:
  Please refer to the diagram at right.
- Package: BGA-560 pins
  (25 mm × 25 mm)

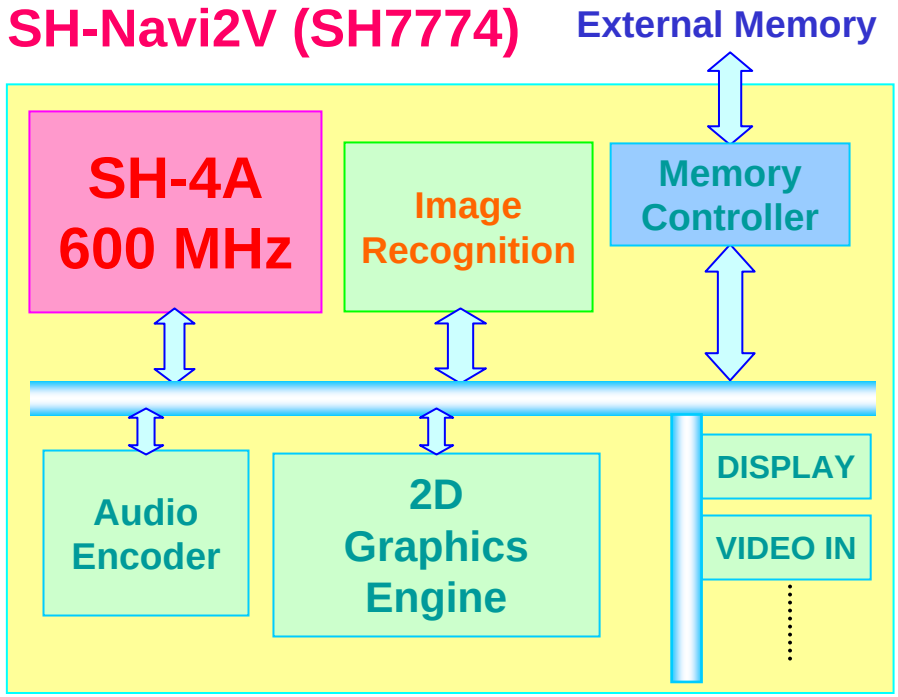


SoC for Car Navigation System SH-Navi2V “SH7774”

- **High performance SoC equipped with the image recognition processing function and various function for car navigation system.**

Product concept





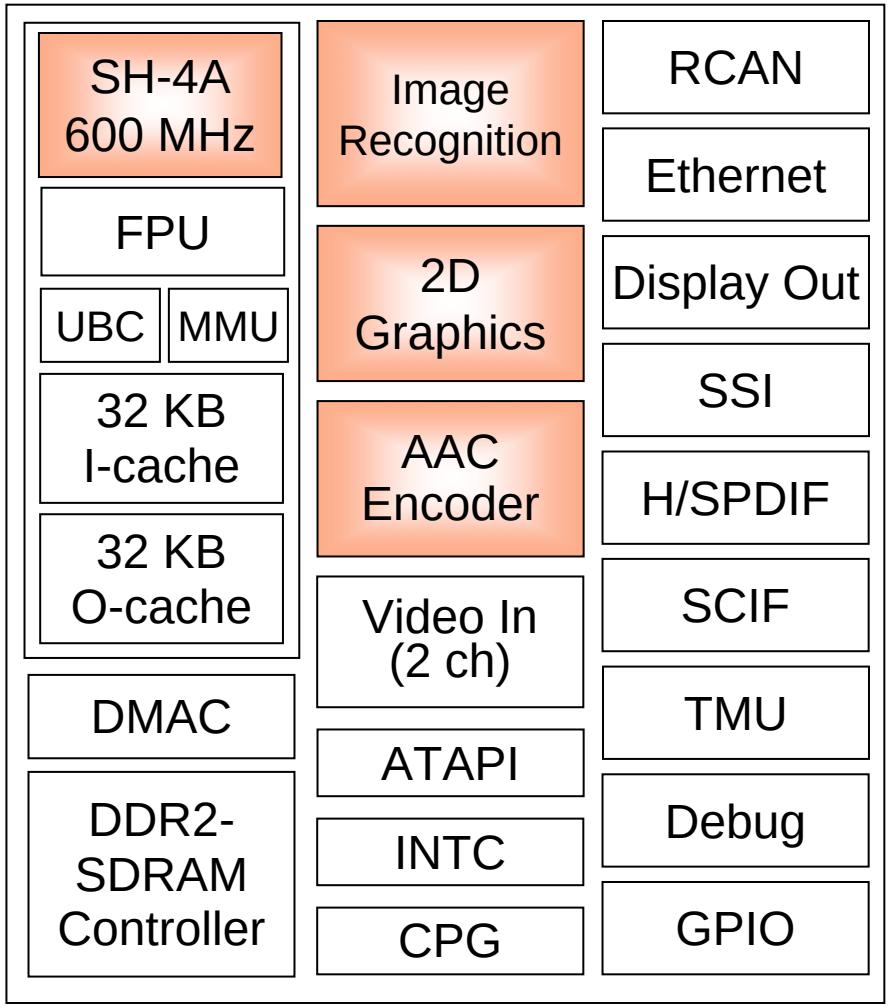
1. World’s first on-chip image recognition processing IP in a car navigation SoC.
2. 600 MHz SH-4A CPU core enabling implementation of high-performance systems for the next generation.
3. Comprehensive range of peripheral functions for next -generation in-vehicle information terminals.

SH7774 Overview

SH7774

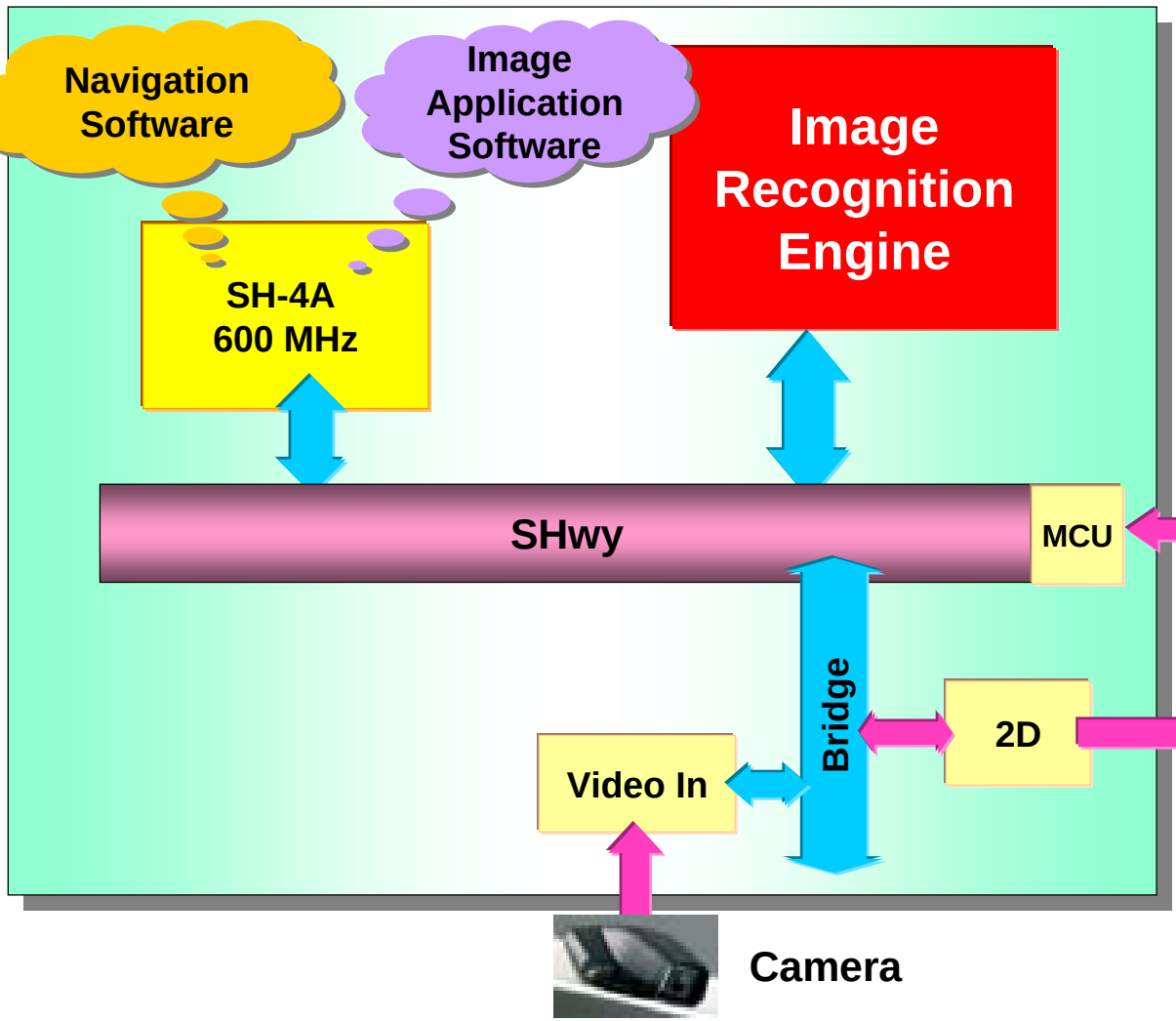
Features

- Max. internal operating frequency of
  SH-4A core: 600 MHz
- Power supply voltage:
  3.3 V (I/O), 1.8 V (DDR), 1.1 V (Core)
- Performance:
  1080 MIPS@600 MHz
- Cache:
  32-KB 4-way set associative (I-, O-cache)
- Memory: DDR2 SDRAM I/F
- 2D Graphics Engine
- Display:
  WVGA 832 dots × 496 dots (16-bit pixel)
- Peripheral functions:
  Please refer to the diagram at right.
- Package: BGA-554 pins
  (29 mm × 29 mm)



SH-Navi2V “SH7774” Image Recognition Engine

The seamless process is available between CPU and Image Engine

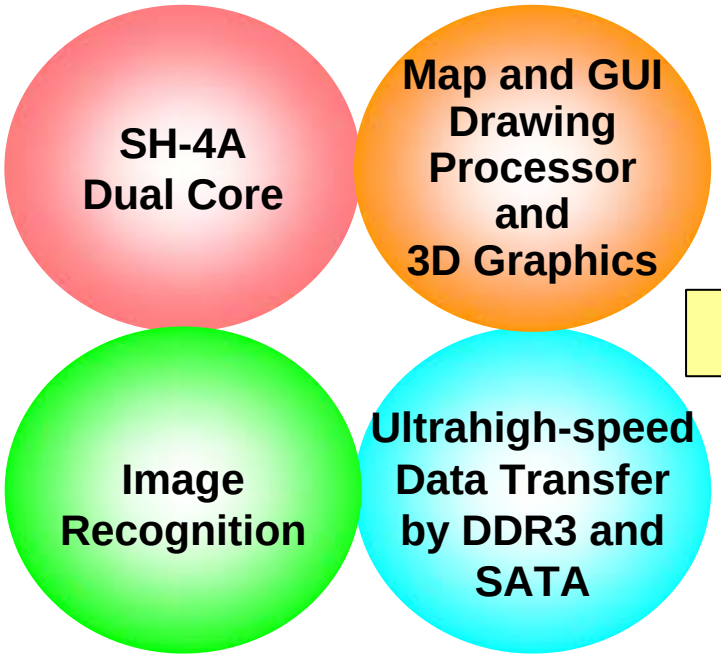


Processing result of Lane Recognition by SH7774

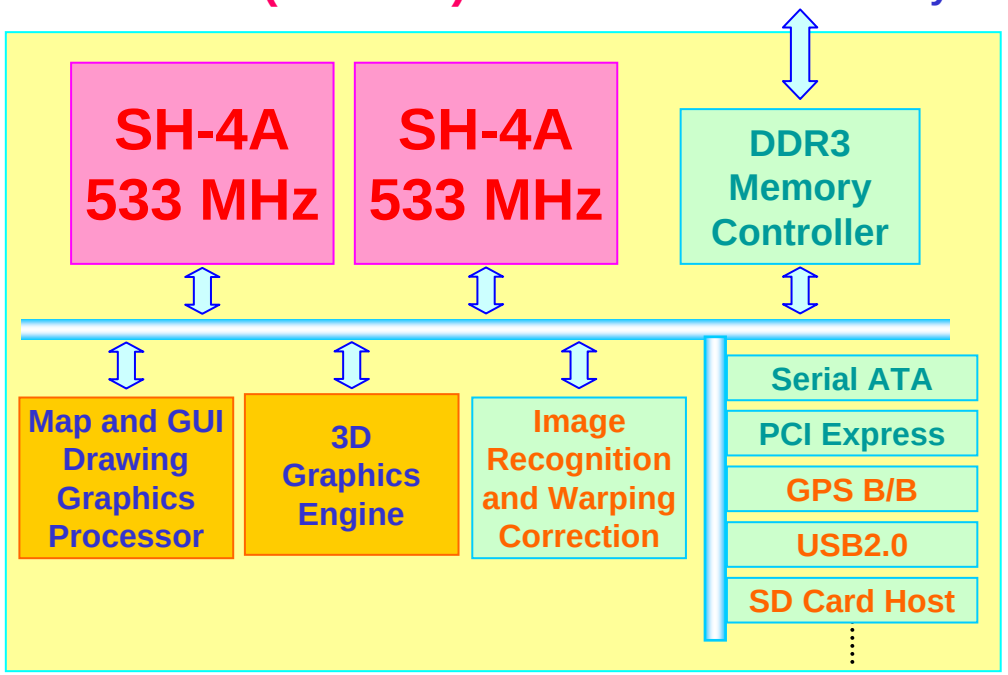
SoC for Car Navigation System SH-Navi3 “SH7776”

- **High performance SoC equipped with SH-4A dual core for High-end car navigation system.**

Product concept



SH-Navi3 (SH7776)



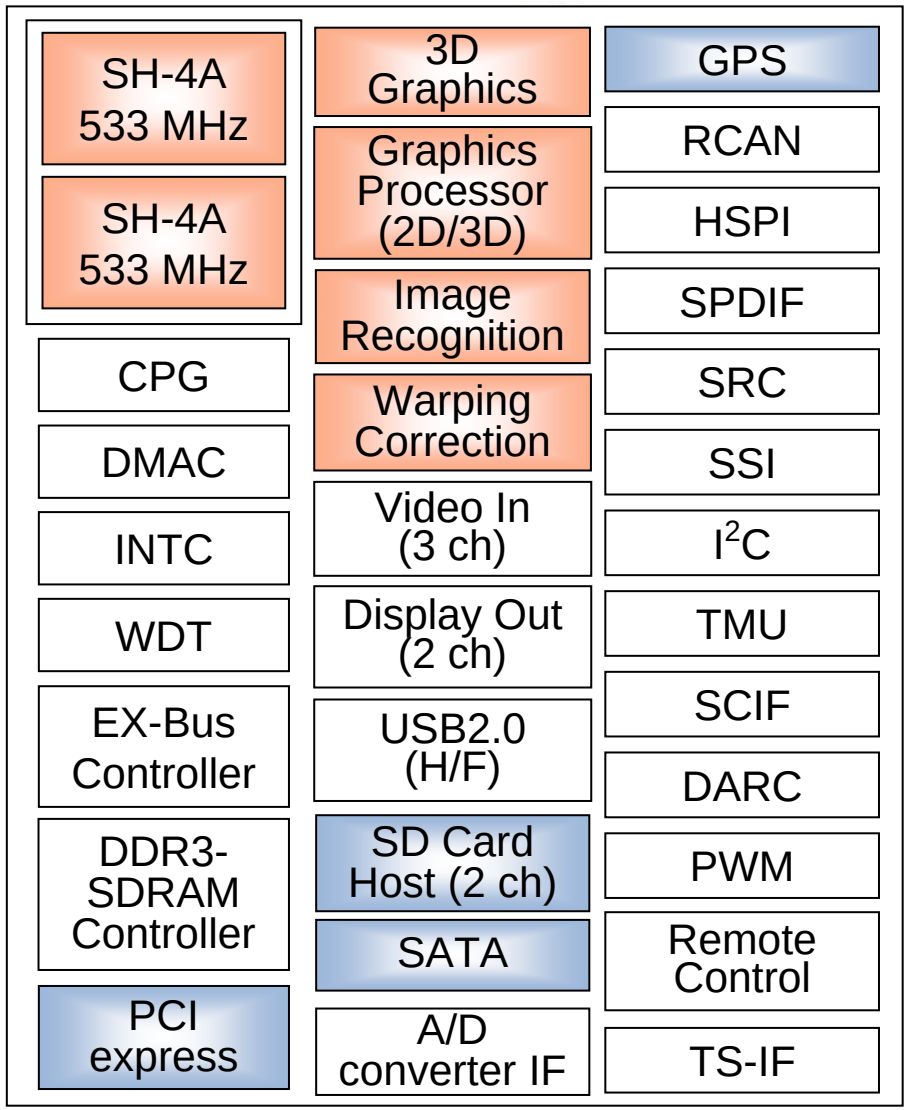
1. Dual high-performance SH-4A CPU cores for superior processing power of 1920 MIPS
2. On-chip Graphics Processor optimized for Map and GUI Drawing and 3-D Graphics Engine achieving high-speed and wide variety of drawing function.
3. Comprehensive range of peripheral functions for car information systems such as Image Recognition processing IP and Wrapping Correction module.
4. On-chip DDR3-SDRAM memory interface, Serial ATA interface, and PCI Express interface for ultrahigh-speed data transfers

SH7776 Overview

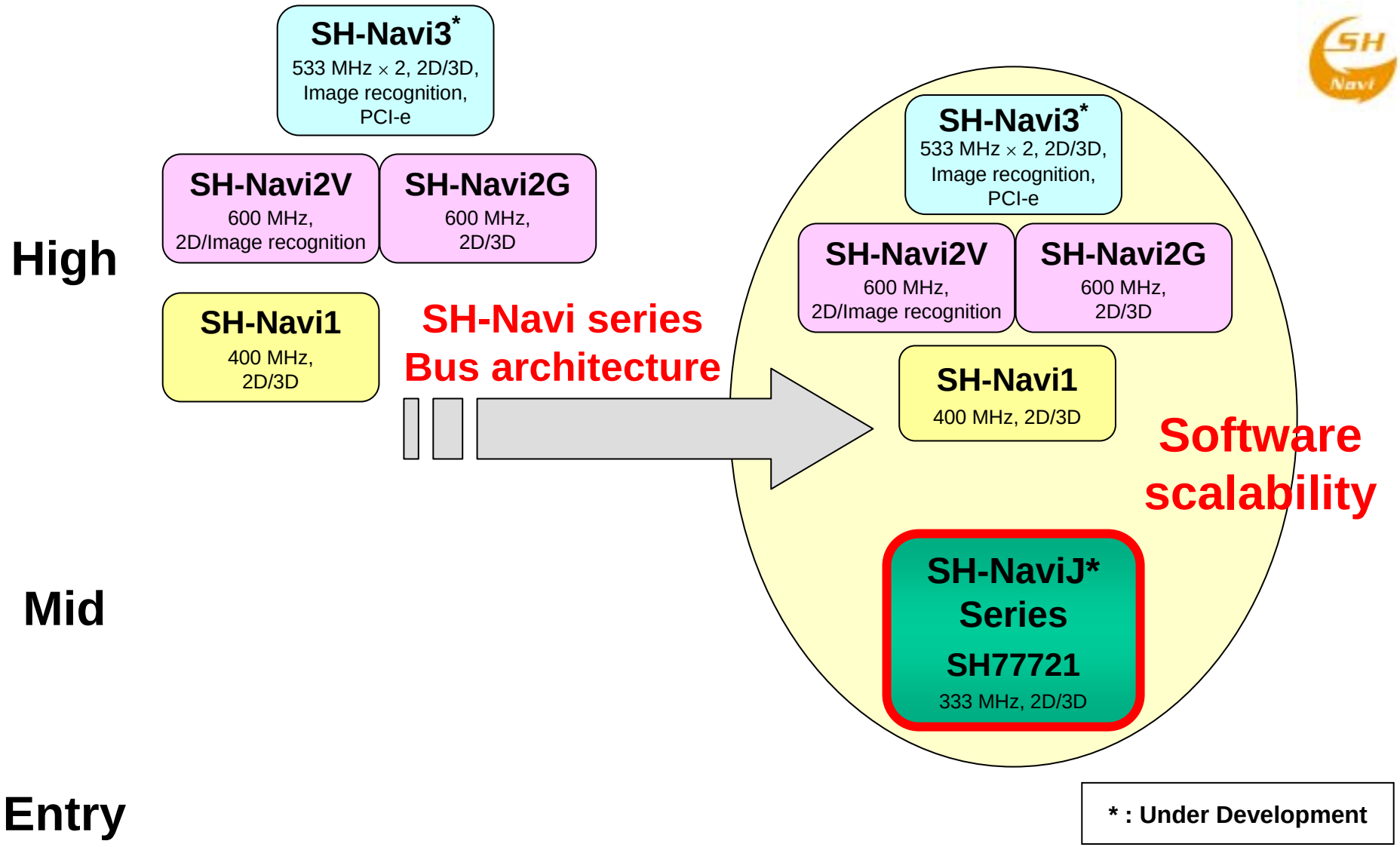
SH7776

Features

- Max. internal operating frequency of
  SH-4A core: 533 MHz × 2
- Power supply voltage:
  3.3 V (I/O), 1.5 V (DDR), 1.25 V (Core)
- Performance:
  1920 MIPS (Dhrystone)@533 MHz
- 2-way superscalar, 7-stage pipeline
- Cache:
  32-KB 4-way set associative (I-, O-cache)
- Memory: DDR3 SDRAM I/F
- Renesas Graphics Processor (2D, 3D)
- 3D Graphics Engine
- Display:
  WXGA 1280 dots × 768 dots (16-bit pixel)
- Peripheral functions:
  Please refer to the diagram at right.
- Package: BGA-653 pins
  (25 mm × 25 mm, 0.8-mm pitch)

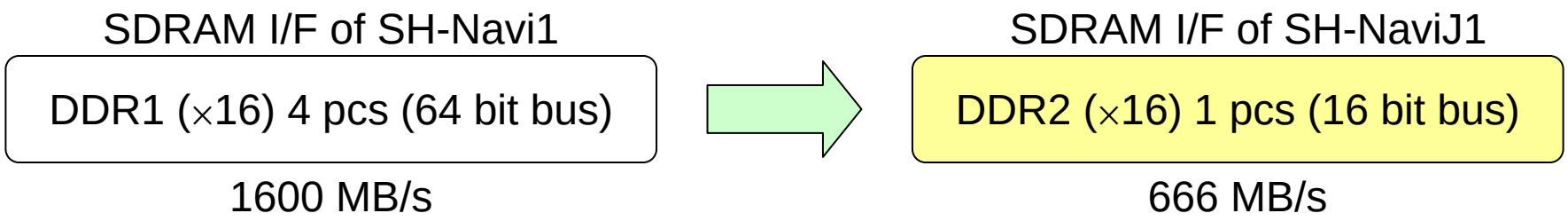


SH-Navi Series Roadmap (Entry-High-End)



New SoC SH-NaviJ1 “SH77721” for Low-End to Middle-Range Car Navigation Systems

1. The optimized specification for an entry CIS model
   - Enhanced Renesas Graphics Processor
   - USB 2.0 High speed
   - Add SD Card host Interface
   - CPU 333 MHz, low power consumption
   - Smaller package
2. Save the software development cost
   - Software scalability can use software property of SH-Navi series, (e.g. common 2D Graphics and peripheral modules)
3. Save the external SDRAM cost.

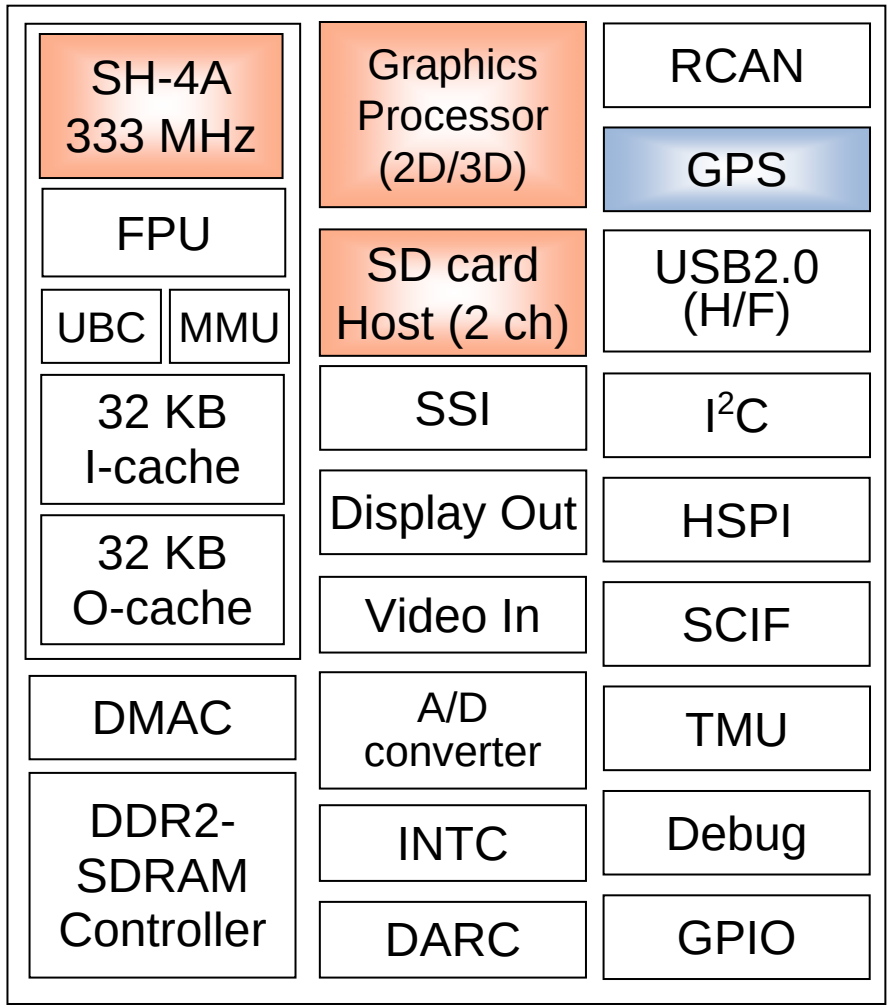


SH77721 Overview

SH77721

Features

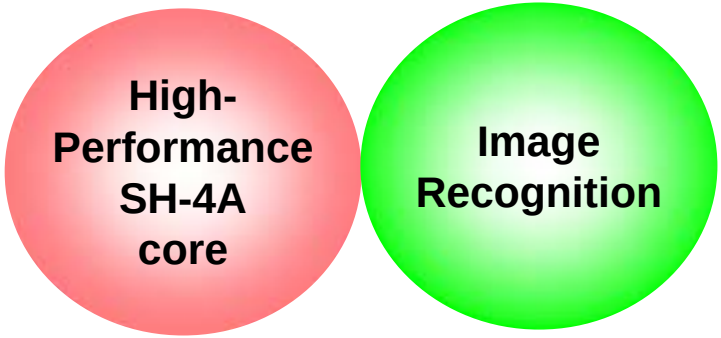
- Max. internal operating frequency of
  SH-4A core: 333 MHz
- Power supply voltage:
  3.3 V (I/O), 1.8 V (DDR), 1.25 V (Core)
- Performance:
  599 MIPS @333 MHz
- Cache:
  32-KB 4-way set associative
  (I-, O-cache)
- Memory: DDR2 SDRAM I/F
- Renesas Graphics Processor (2D/3D)
- Display:
  WVGA 832 dots × 496 dots (16-bit pixel)
- Peripheral functions:
  Please refer to the diagram at right.
- Package: BGA-440 pins
  (23 mm × 23 mm)

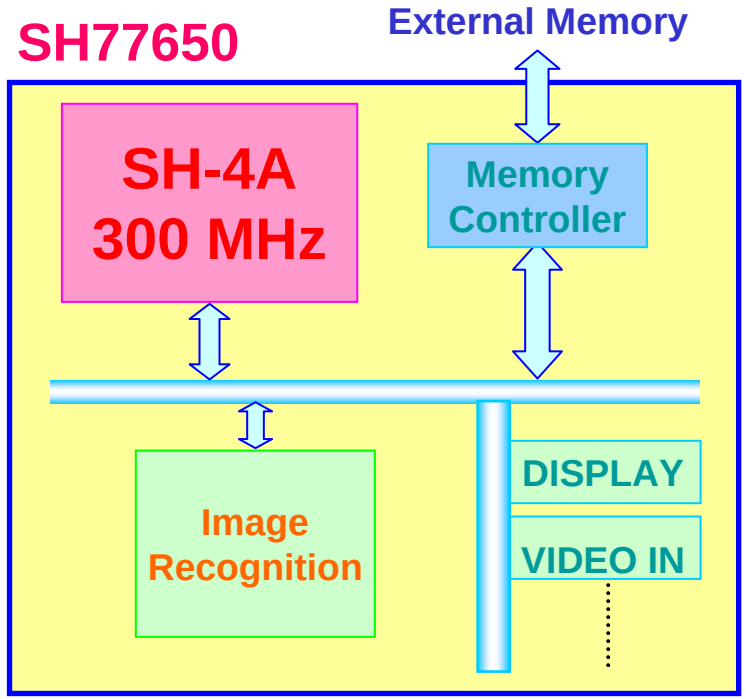


“SH77650” Specialized SoC for Automotive Image Recognition Processing

- 1 chip solution for image recognition system

Product concept





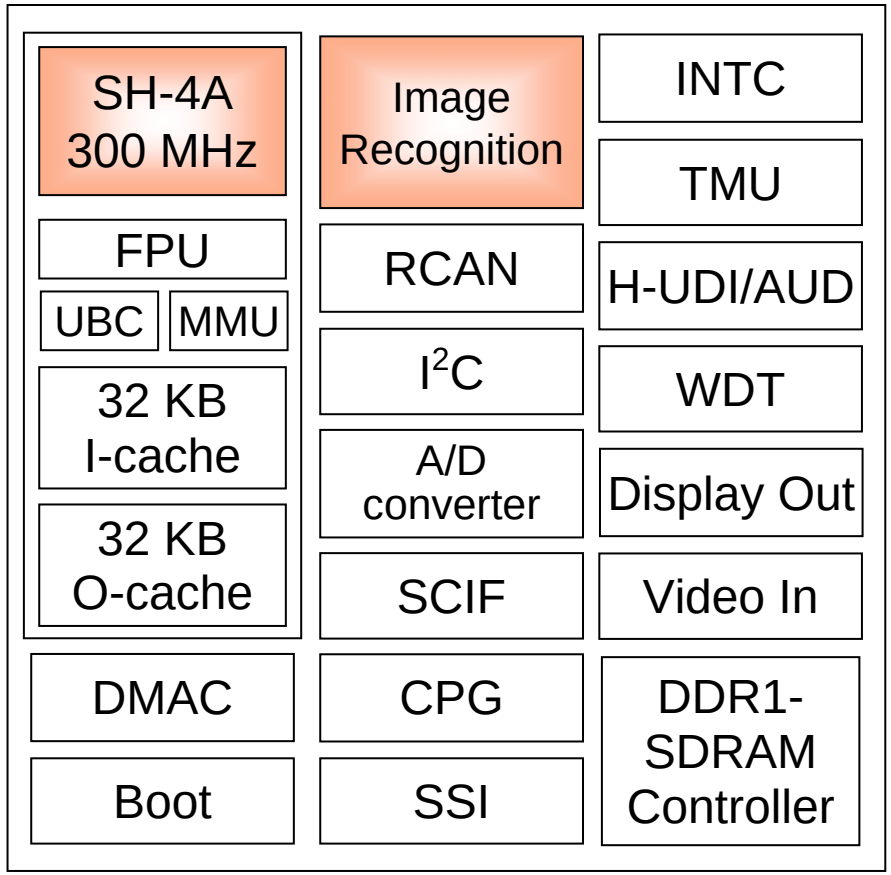
1. High-performance image recognition processing IP
2. SH-4A CPU core operating at 300 MHz to enable actualization of high-performance systems
3. A variety of peripheral functions for automotive image recognition applications

SH77650 Overview

SH77650

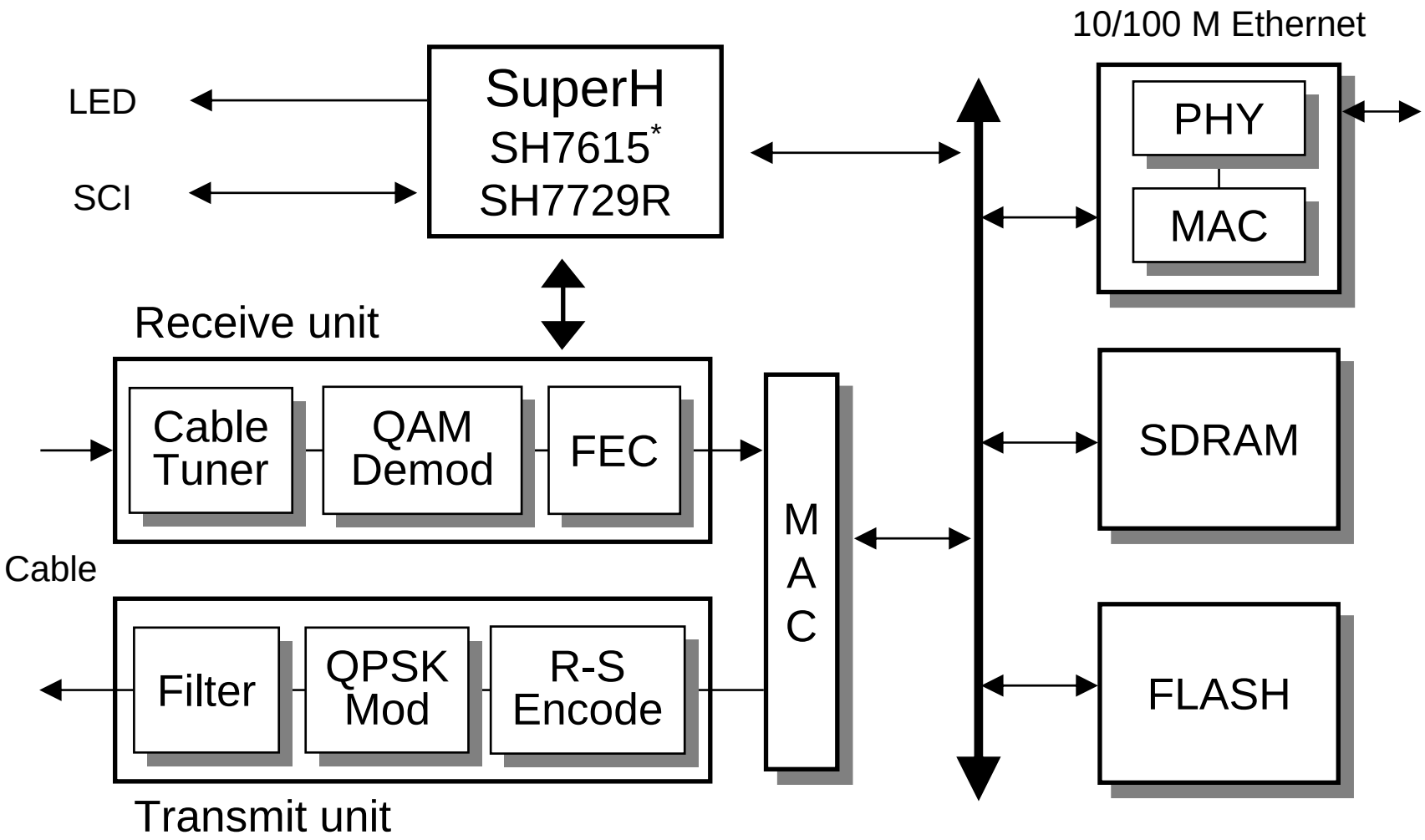
Features

- Max. internal operating frequency of
  SH-4A core: 300 MHz
- Power supply voltage:
  3.3 V (I/O), 2.5 V (DDR), 1.2 V (Core)
- Performance:
  540 MIPS@300 MHz
- Image recognition engine
- Cache:
  32-KB 4-way set associative (I-, O-cache)
- Memory: DDR1 SDRAM I/F
- Internal RAM 256 KB
- Peripheral functions:
  Please refer to the diagram at right.
- Package: BGA-376 pins
  (19 mm × 19 mm)



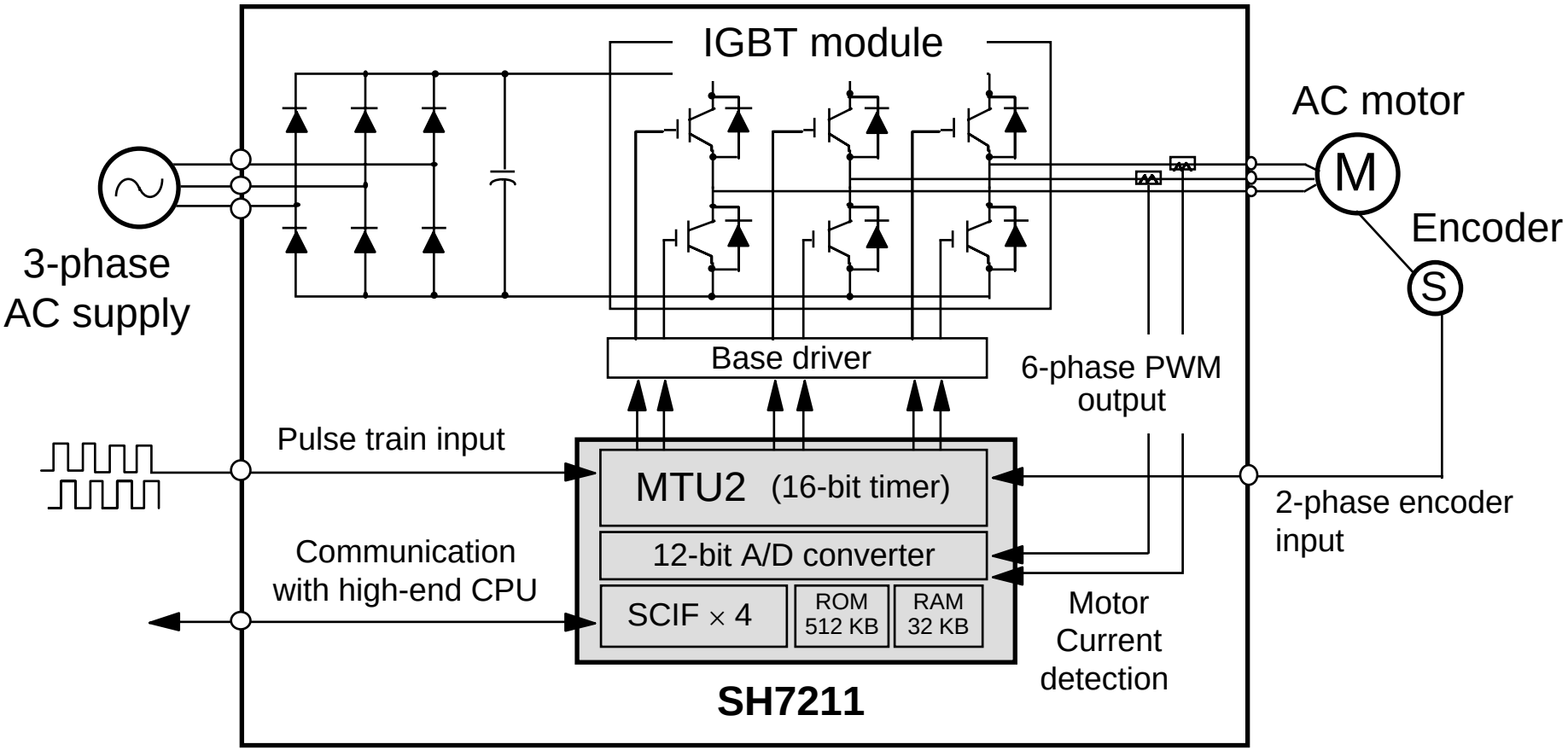
SuperH RISC engine System Application

Configuration Example of the Cable Modem



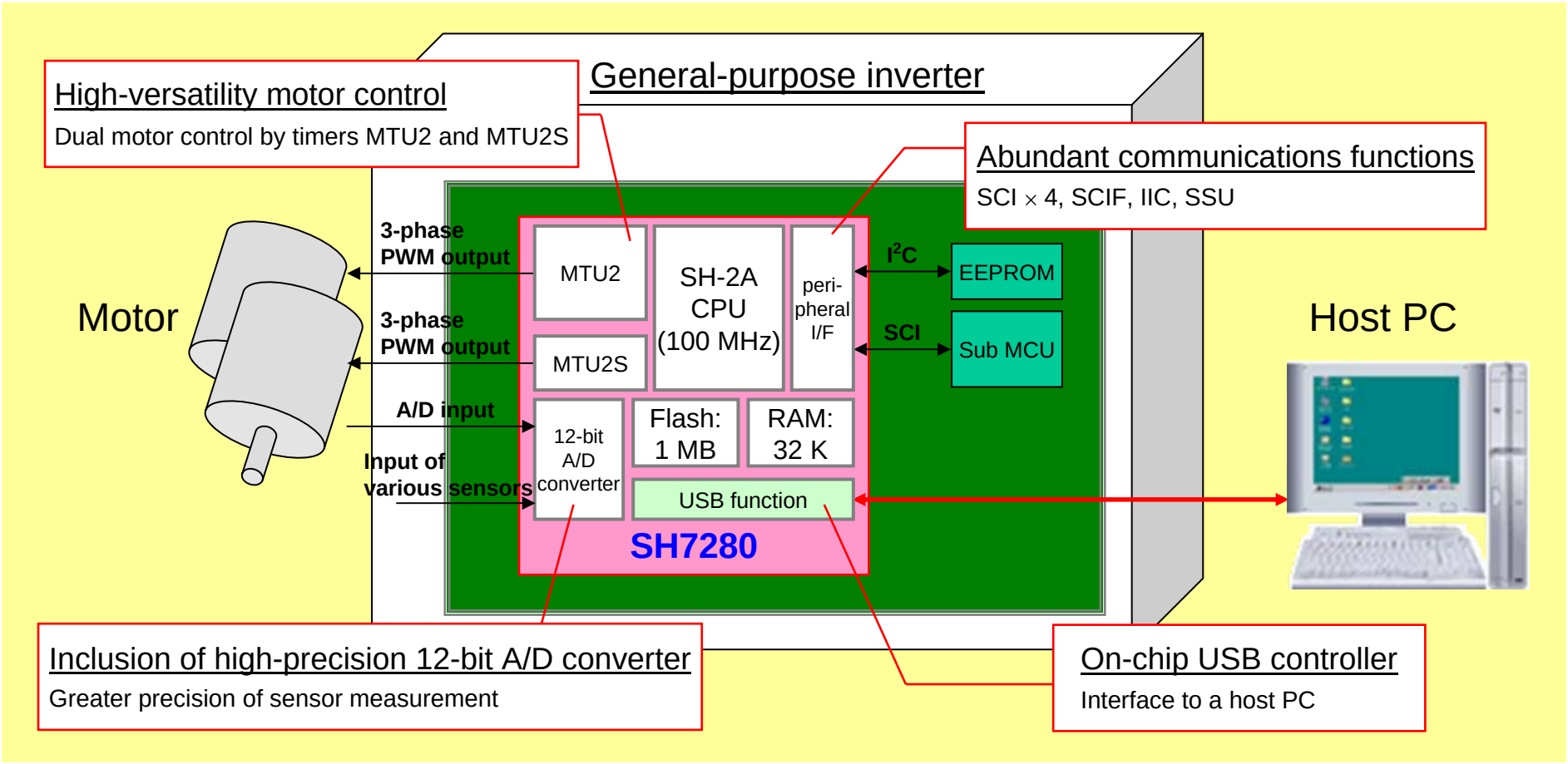
*: SH7615 incorporates Ether MAC.

Configuration Example of the AC Servo Control System



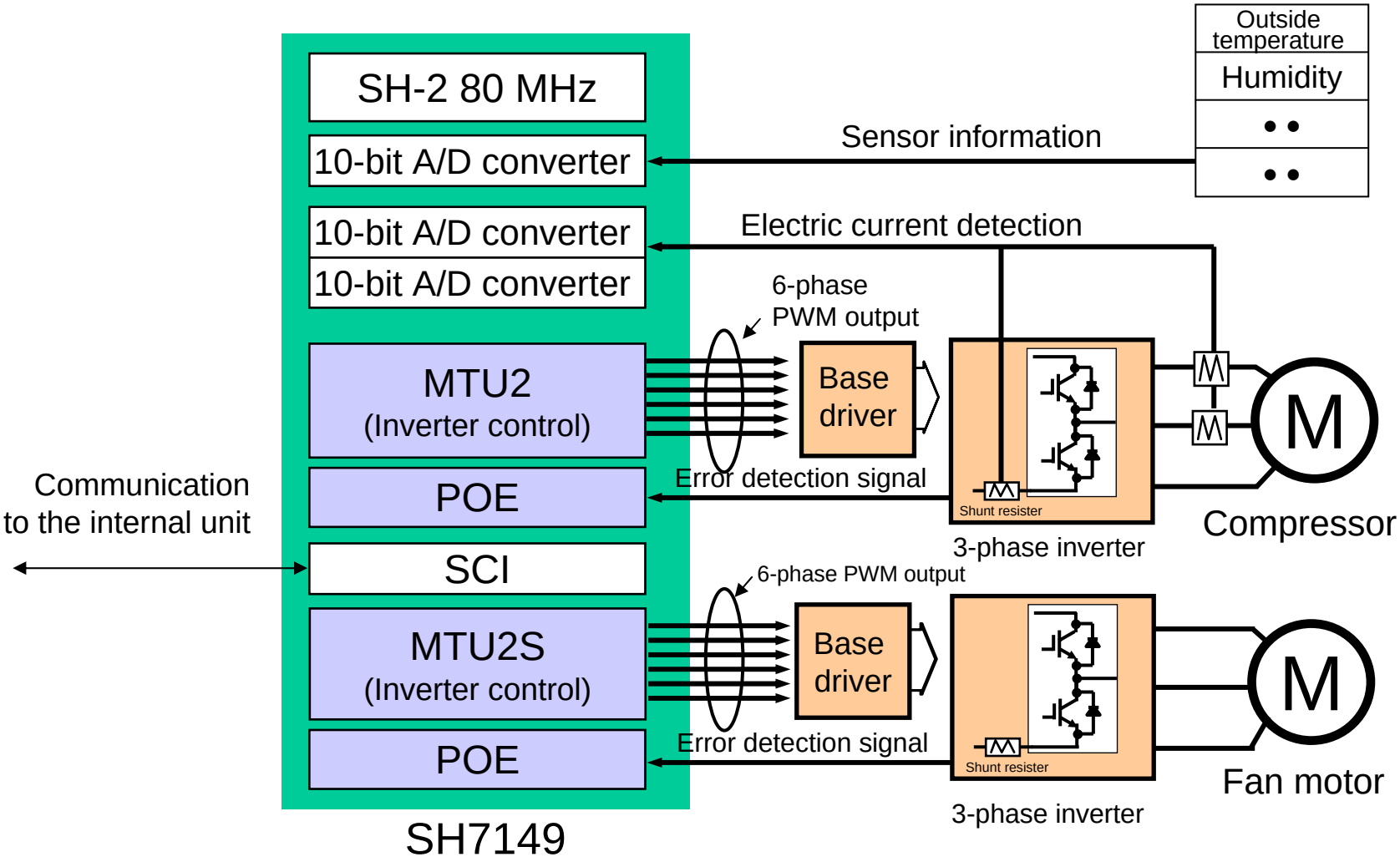
NEW General-Purpose Inverter: Example of System Configuration

High-precision and high functionality inverter system can be realized by enhanced-performance SH-2A CPU core, large-capacity flash memory with up to 1 MB, and timers (MTU2 and MTU2S) for motor control.
USB controller is also included, which enables interface to a host PC.

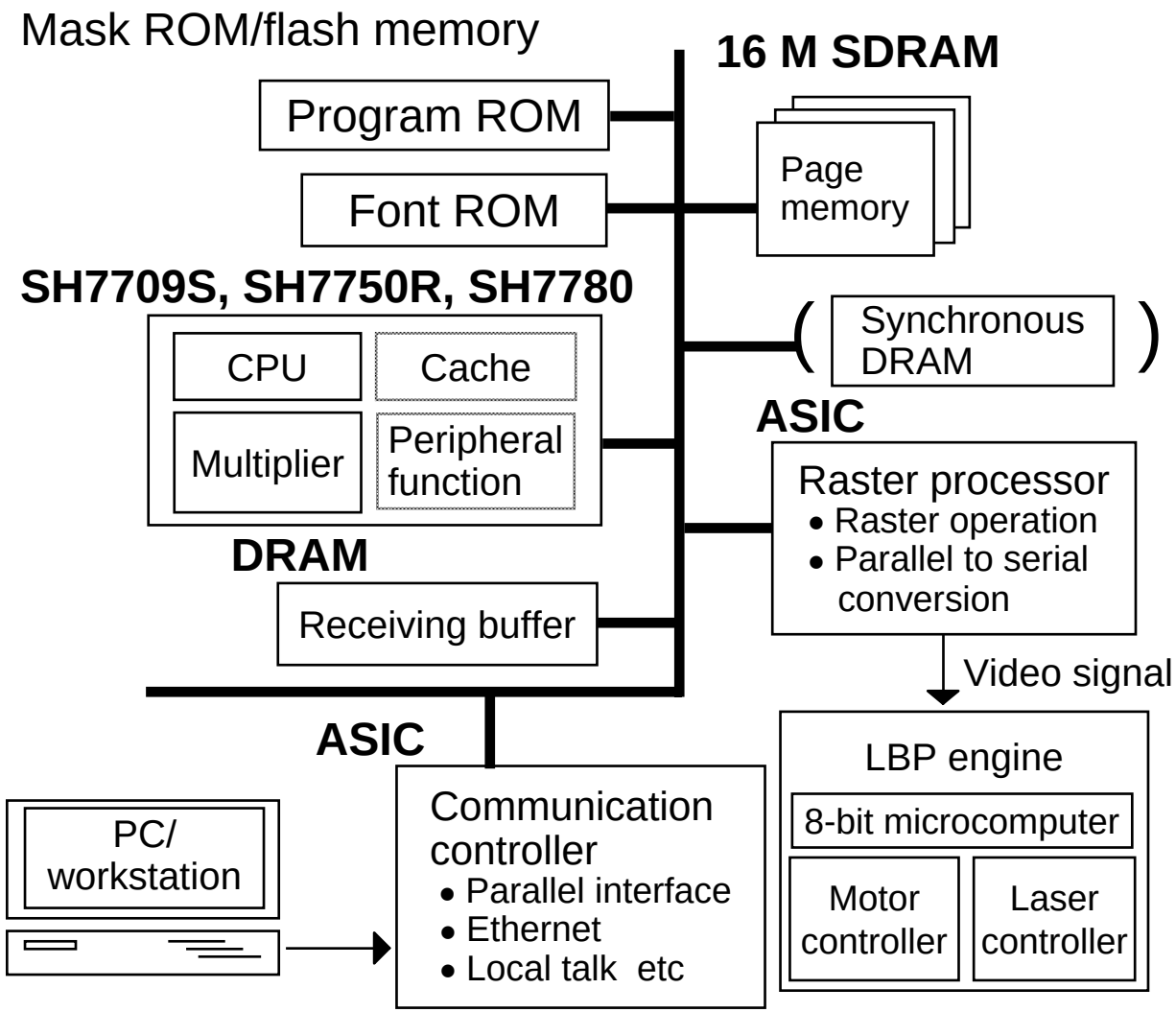


Application Example Using the SH7149

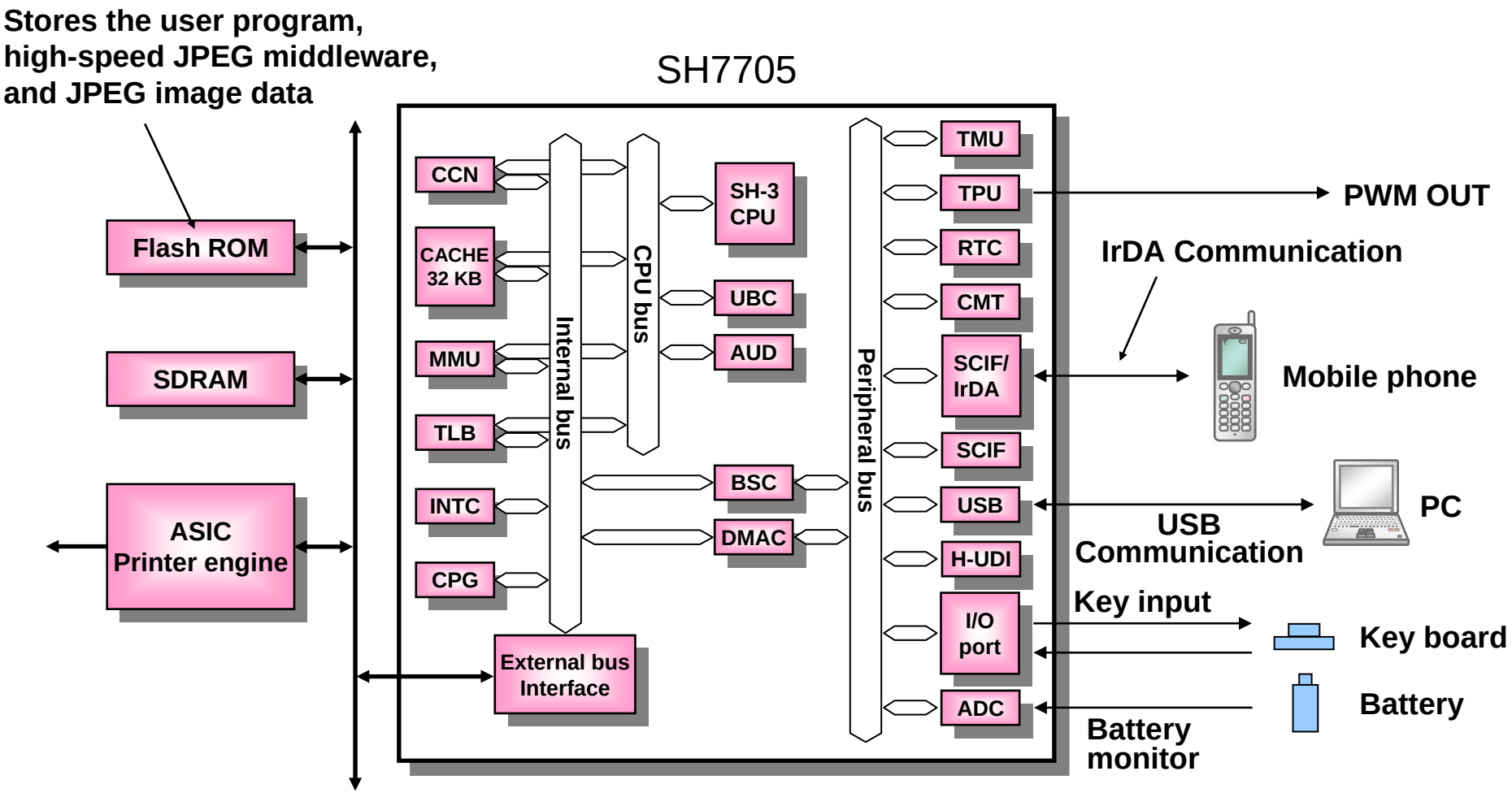
- Controlling the external unit of air conditioner with a single chip -



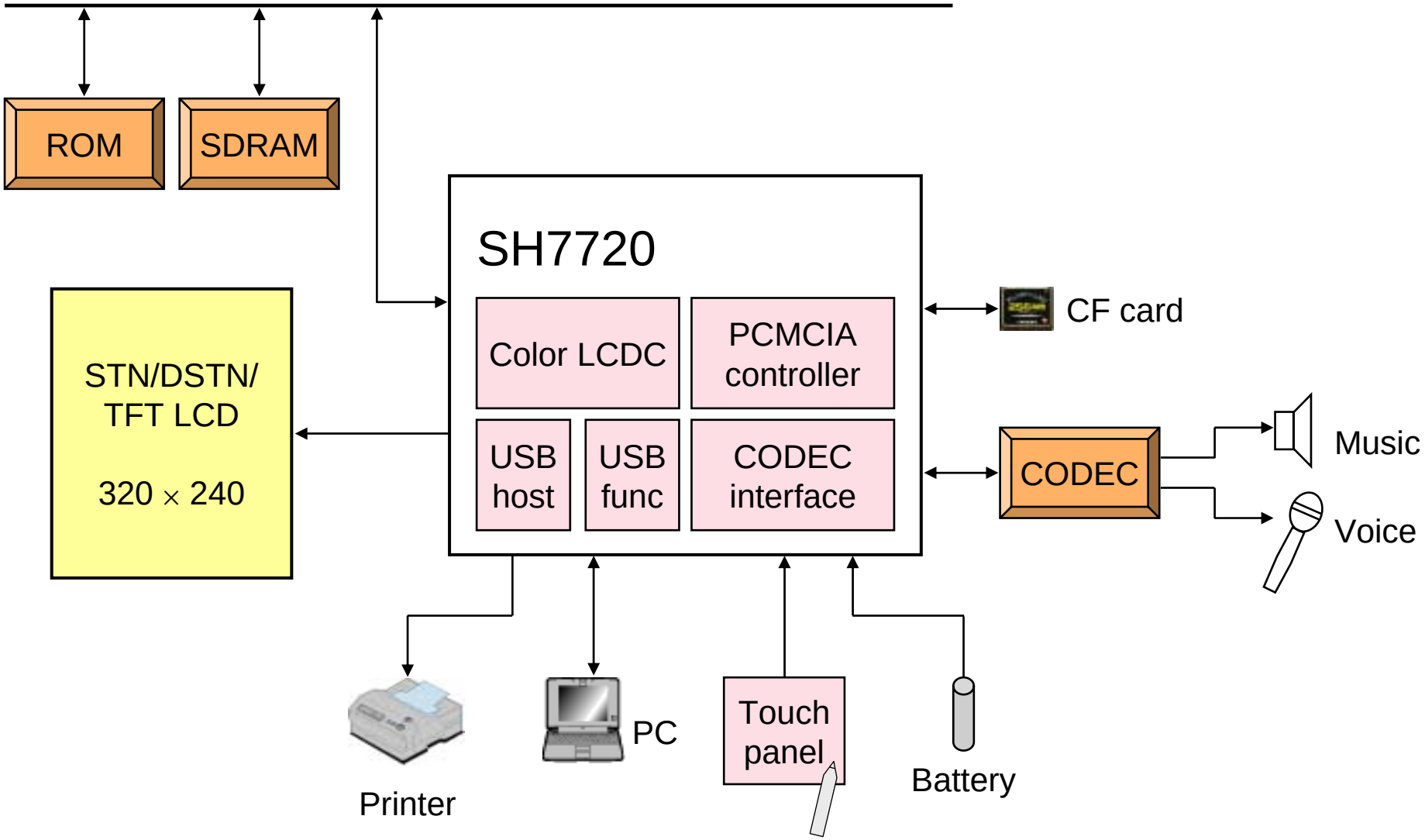
Configuration Example of the Page Printer System



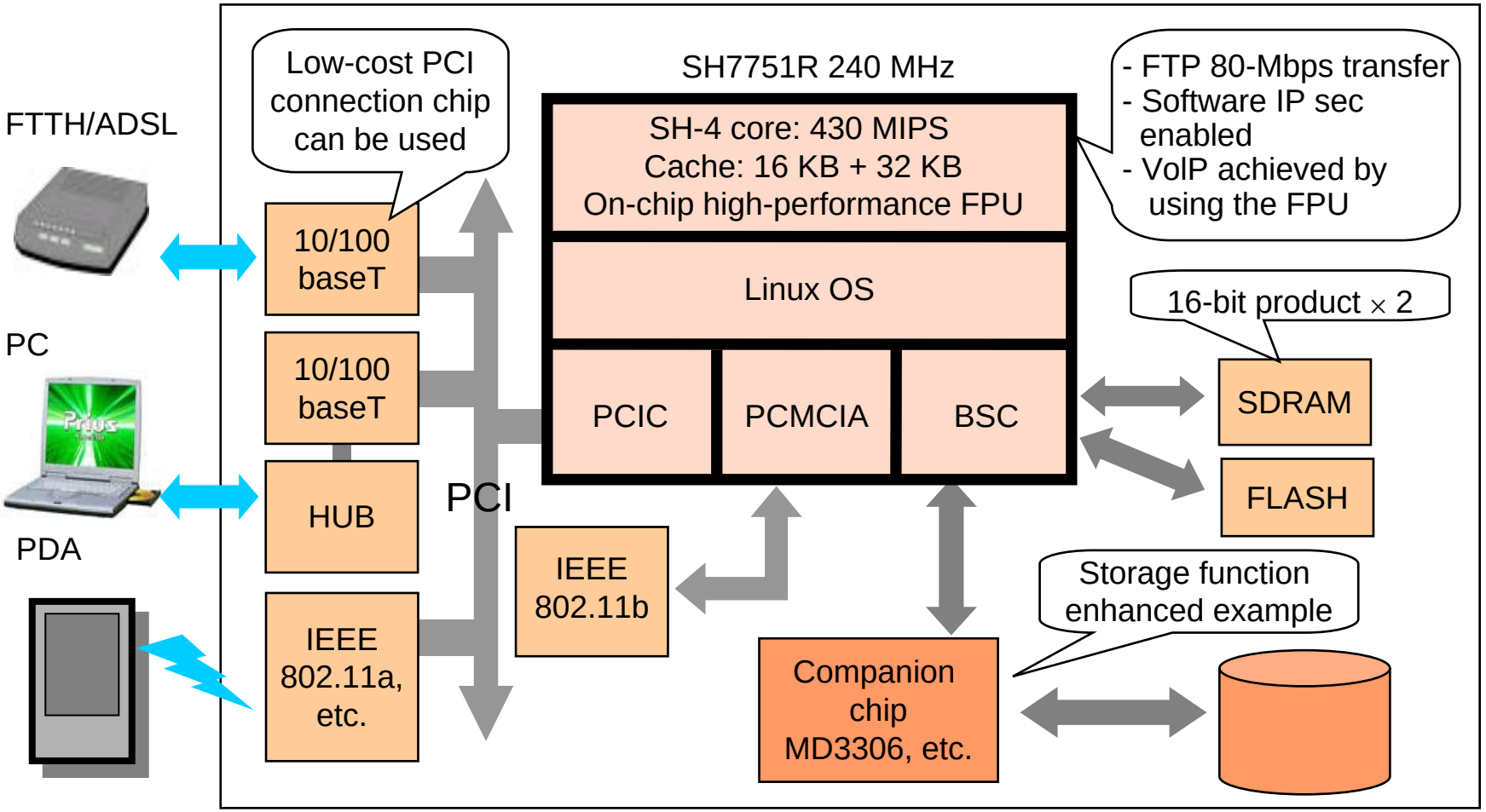
Configuration Example of the Compact Printer System



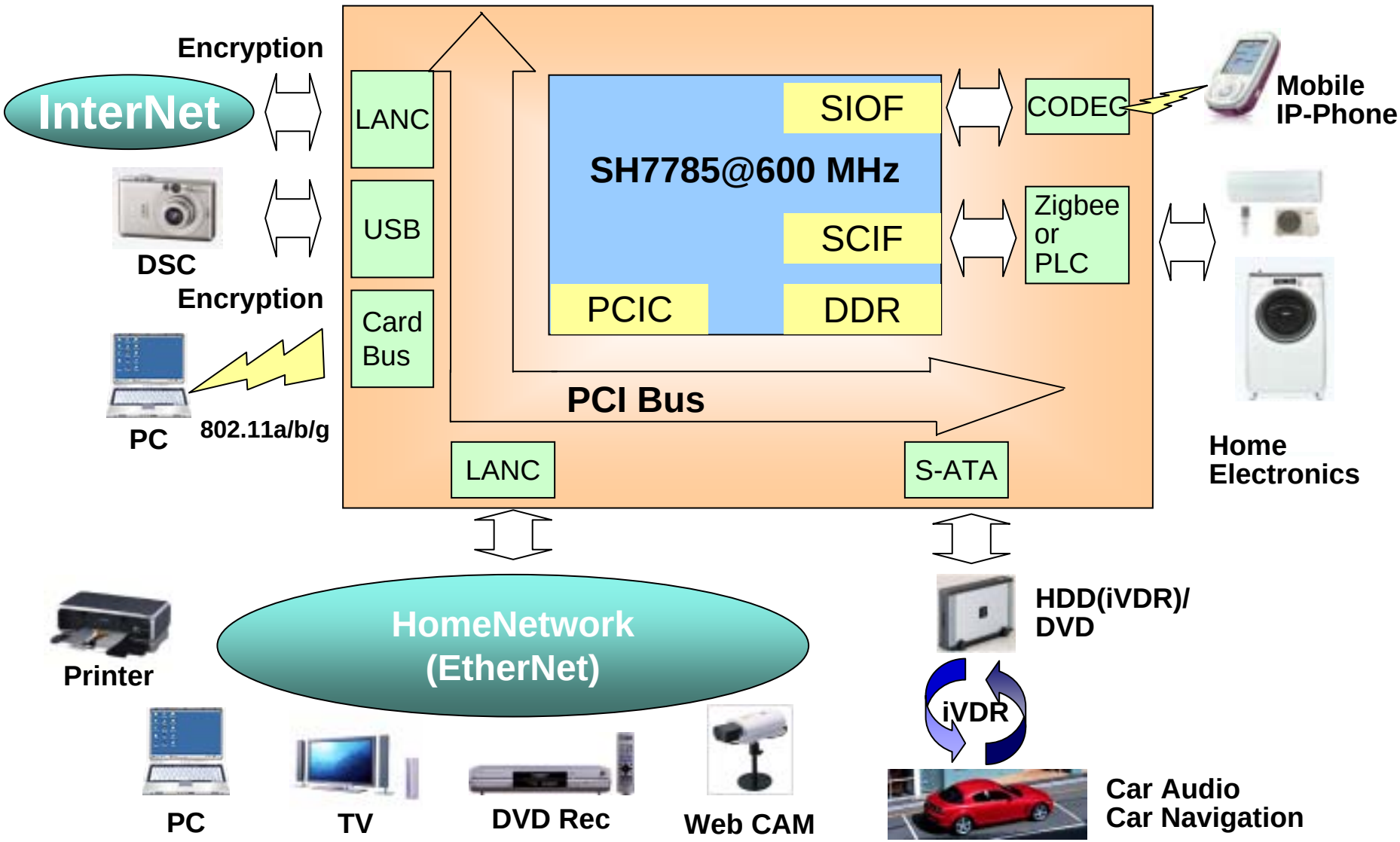
Configuration Example of the Portable Information Terminal System



Gateway Configuration Example Using the SH-4

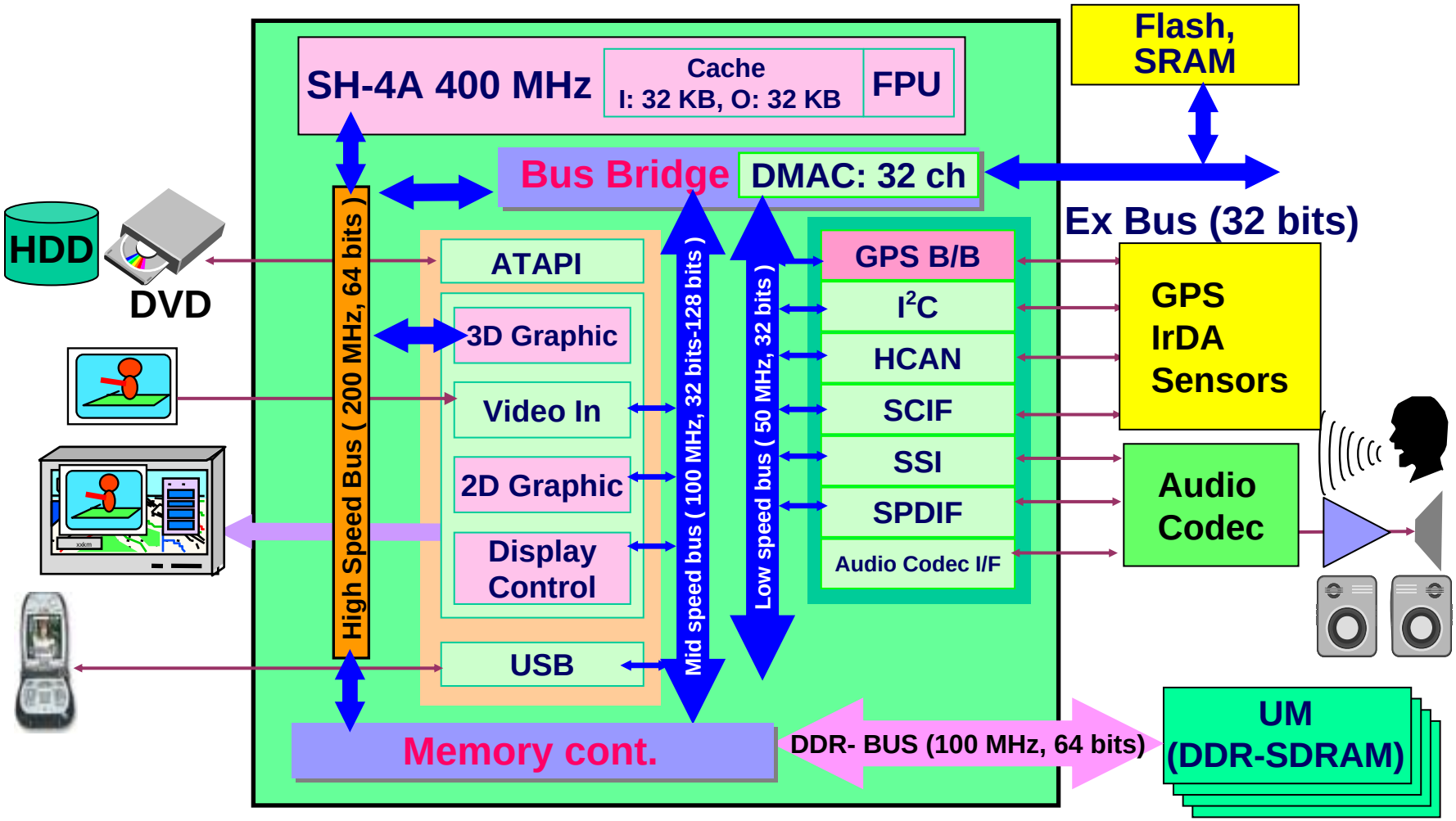


Example of SH7785 Application (Home Server)



Example of Car Navigation System with SH7770

- Fruitful peripheral interface with the separated bus structure.
- Improvement of the cost performance by one-chip solution.



Renesas Technology Corp.